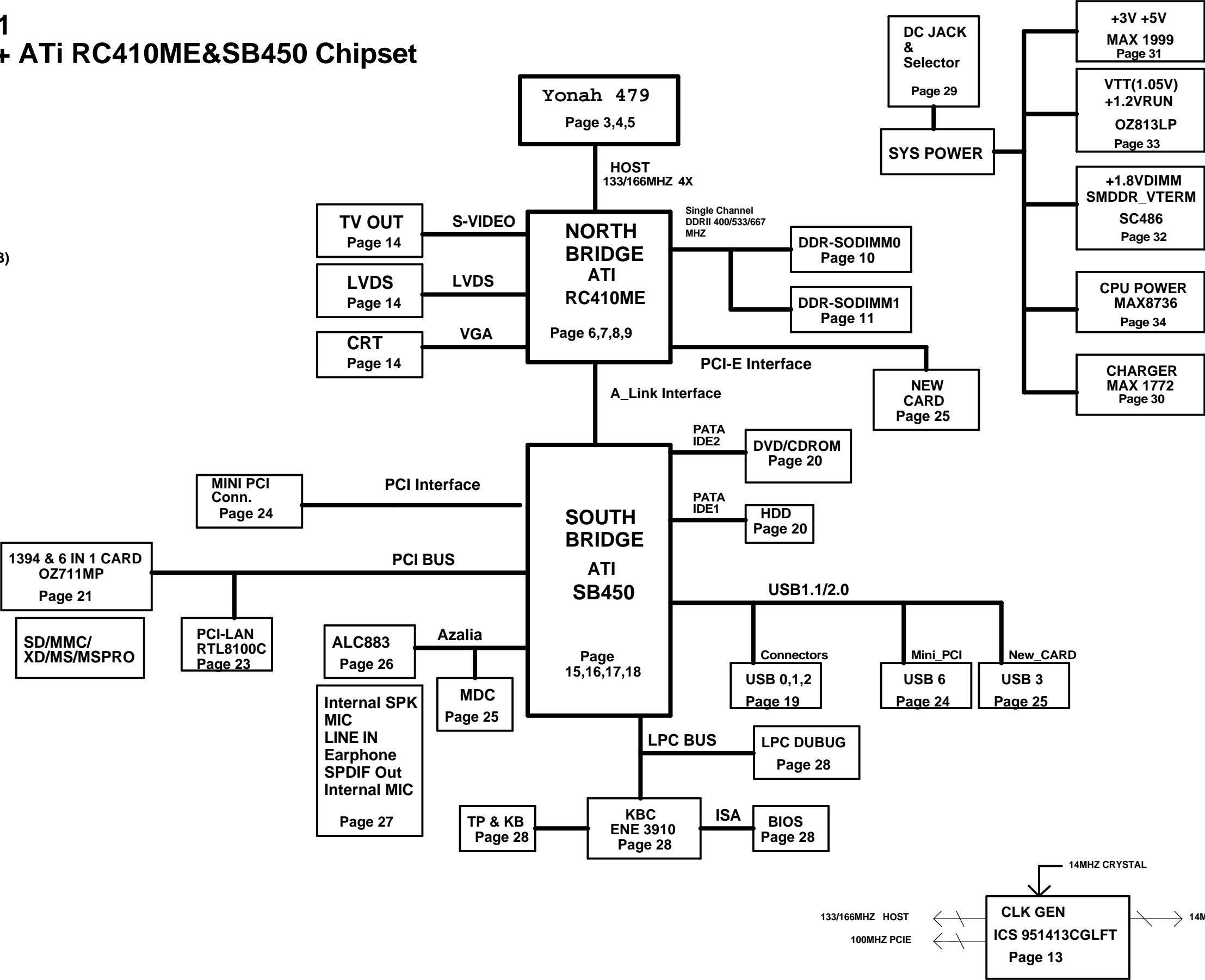


MS-1412 VER:1.1  
Intel Yonah CPU+ ATi RC410ME&SB450 Chipset




- 01:BLOCK DIAGRAM
- 02:PLATFORM
- 03:Yonah-1 CPU (HOST BUS)
- 04:Yonah-2 CPU (POWER/GND)
- 05:Yonah-3
- 06:RC410ME(HOST)
- 07:RC410ME(DDR)
- 08:RC410ME(VIDEO/PCI-E)
- 09:RC410ME(POWER/STRAPS)
- 10:DDR2\_SODIMM0
- 11:DDR2\_SODIMM1
- 12:DDR2\_Termination
- 13:CLOCK GEN(ICS 951413CGLFTB)
- 14:CRT & LVDS & TV CONN
- 15:SB450(AZALIA/USB)
- 16:SB450(PCI/CPU/LPC/RTC)
- 17:SB450(SATA/IDE/POWER)
- 18:SB450(HW STRAPS)
- 19:USB2.0 CON x 3
- 20:HDD & CDROM Connect
- 21:PCI BUS/1394
- 22:CARDBUS
- 23:PCI LAN RTL8100C
- 24:MINI PCI
- 25:NEW CARD& MDC Connect
- 26:CODEC/AMP
- 27:AUDIO/AMP
- 28:KBC/EC/UP
- 29:M\_Battery Select
- 30:M\_Battery Charger
- 31:M\_System Power
- 32:M\_VDDR & +1.8VDIMM
- 33:M\_1.05V,1.2V
- 34:M\_CPU power
- 35:Screw1
- 36:Screw2
- 37:EMI
- 38:KBC POWER SEQUENCE
- 39:POWER SEQUENCE



## Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHORE	Core Voltage for Processor	RUNPWROK
VTT	1.05 rail for Processor & RC410ME I/O	RUND
+1.2VRUN	1.2V powe rail RC410ME, CRT AND LVDS (off in S3-S5)	RUND
+3VRUN	3.3V switched power rail(off in S3-S5)	RUND
+5VRUN	5.0V switched power rail(off in S3-S5)	RUND
+1.8VDIMM	1.8V power rail DDR2 (off in S4-S5)	DIMM_ON
SMDDR_VTERM	0.9V DDR Termination voltage (off in S4-S5)	RUN_ON
+1.8VSUS	1.8V power rail for SB450	+3VSUS
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC

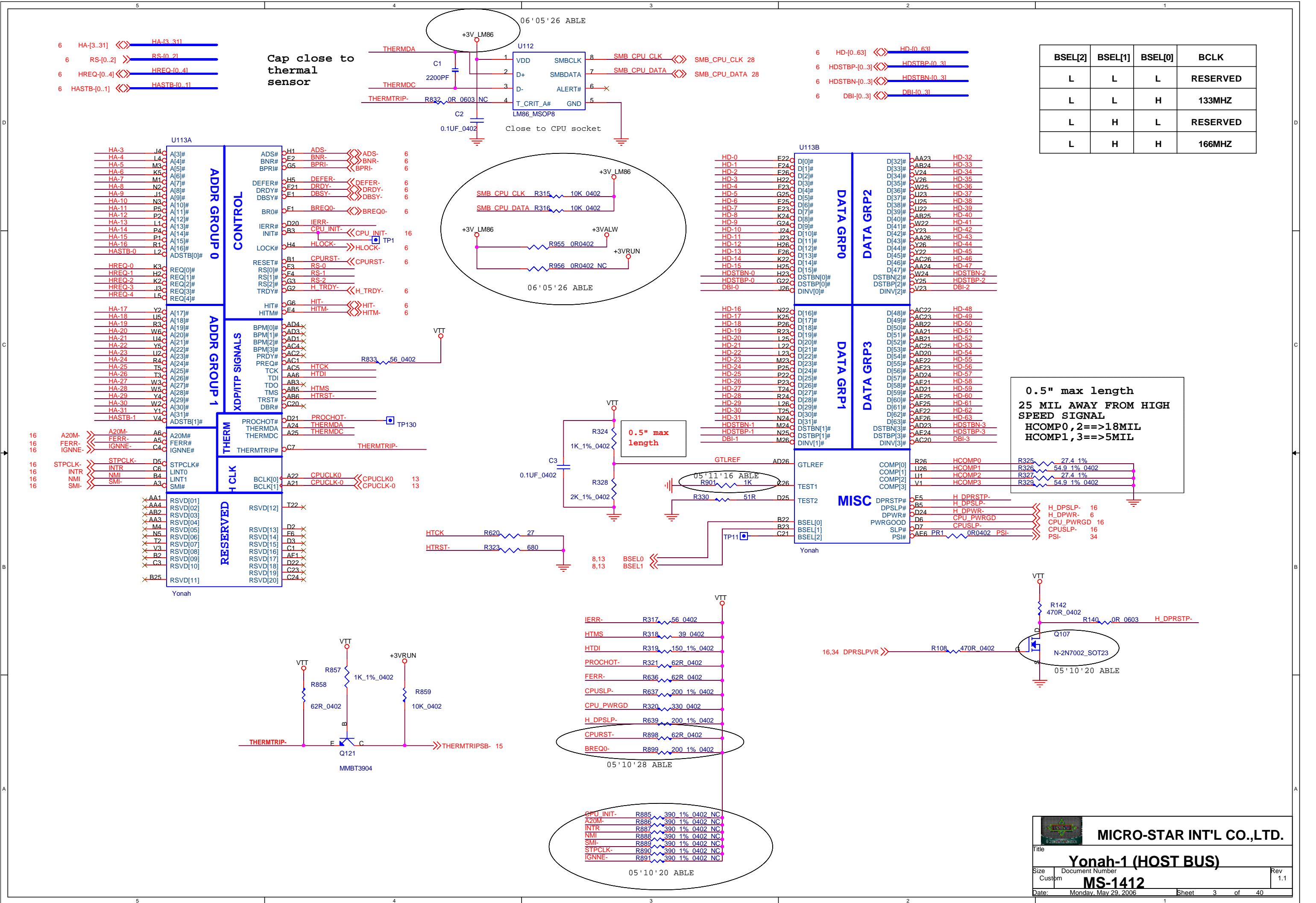
Voltage	Description	Control Signal
ADD5V	5.0V Power rail Audio codec(off in S3-S5)	RUND

 GND	DIGTIAL GROUD	
 AGND	AUDIO GND	
 PGND	POWER Analogy GND	

## POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

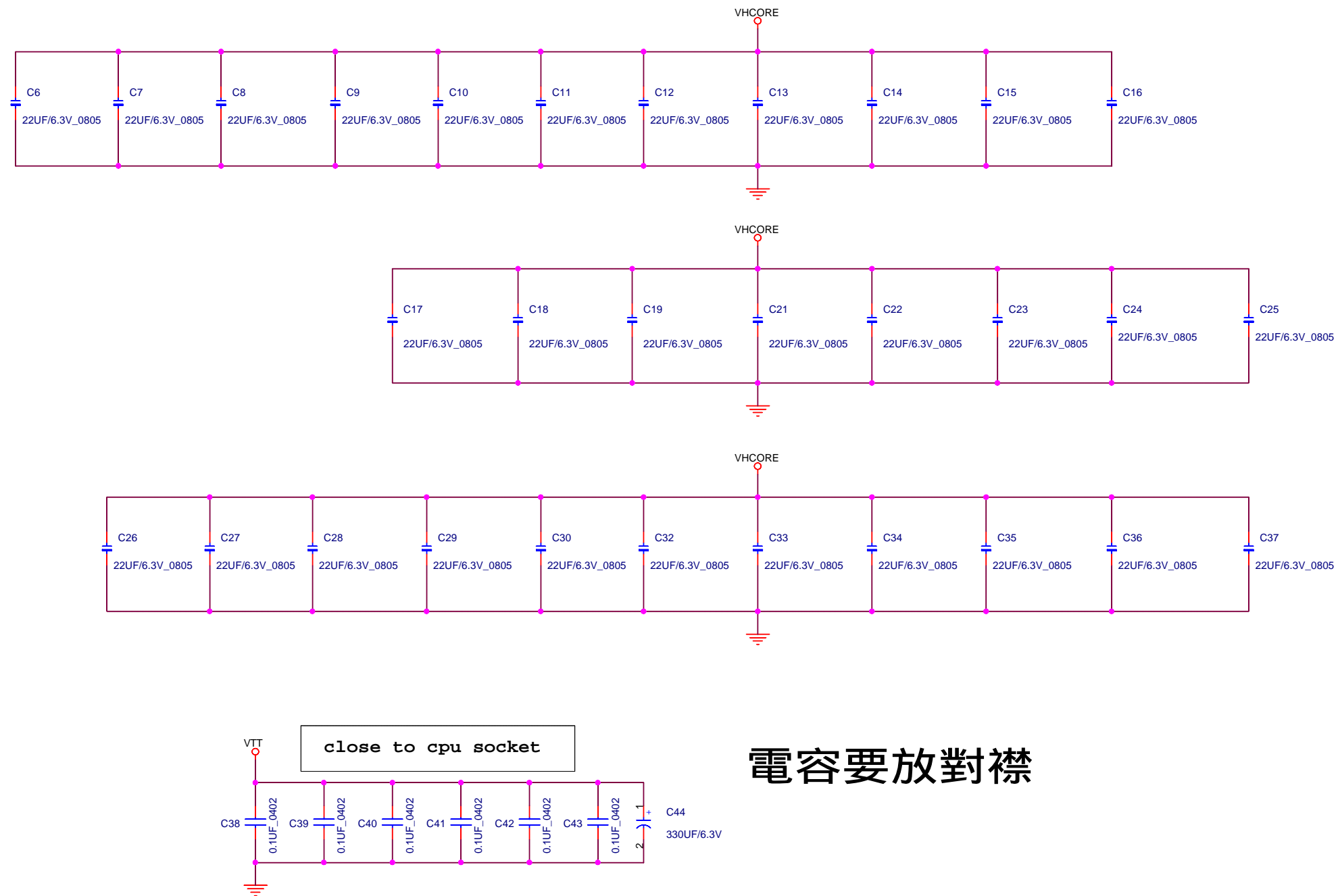
Note : WHEN AC MODE , System turn on then +V\*SUS will always keep high



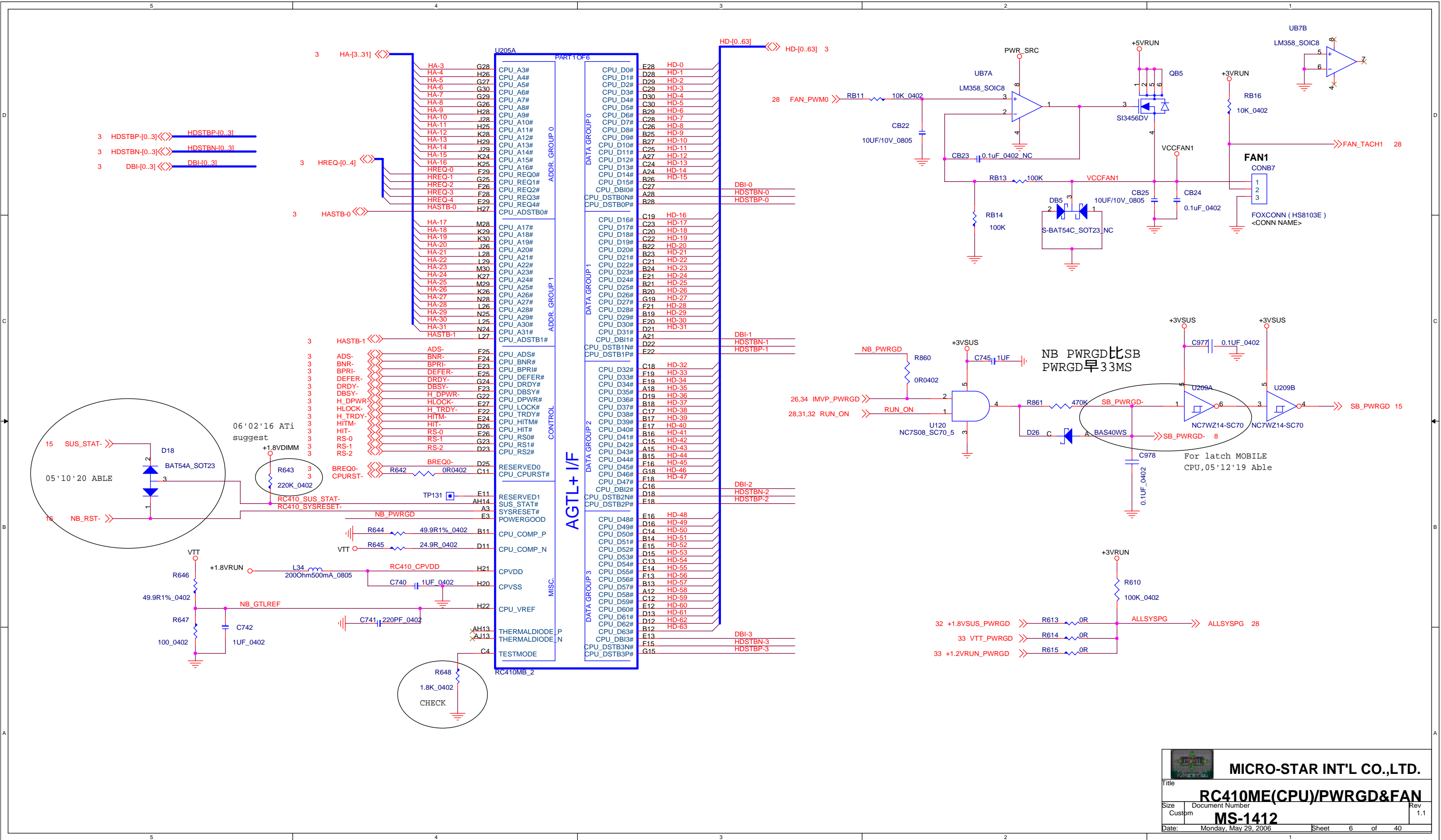
BSEL[2]	BSEL[1]	BSEL[0]	BCLK
L	L	L	RESERVED
L	L	H	133MHZ
L	H	L	RESERVED
L	H	H	166MHZ

0.5" max length  
25 MIL AWAY FROM HIGH  
SPEED SIGNAL  
HCOMP0,2==>18MIL  
HCOMP1,3==>5MIL





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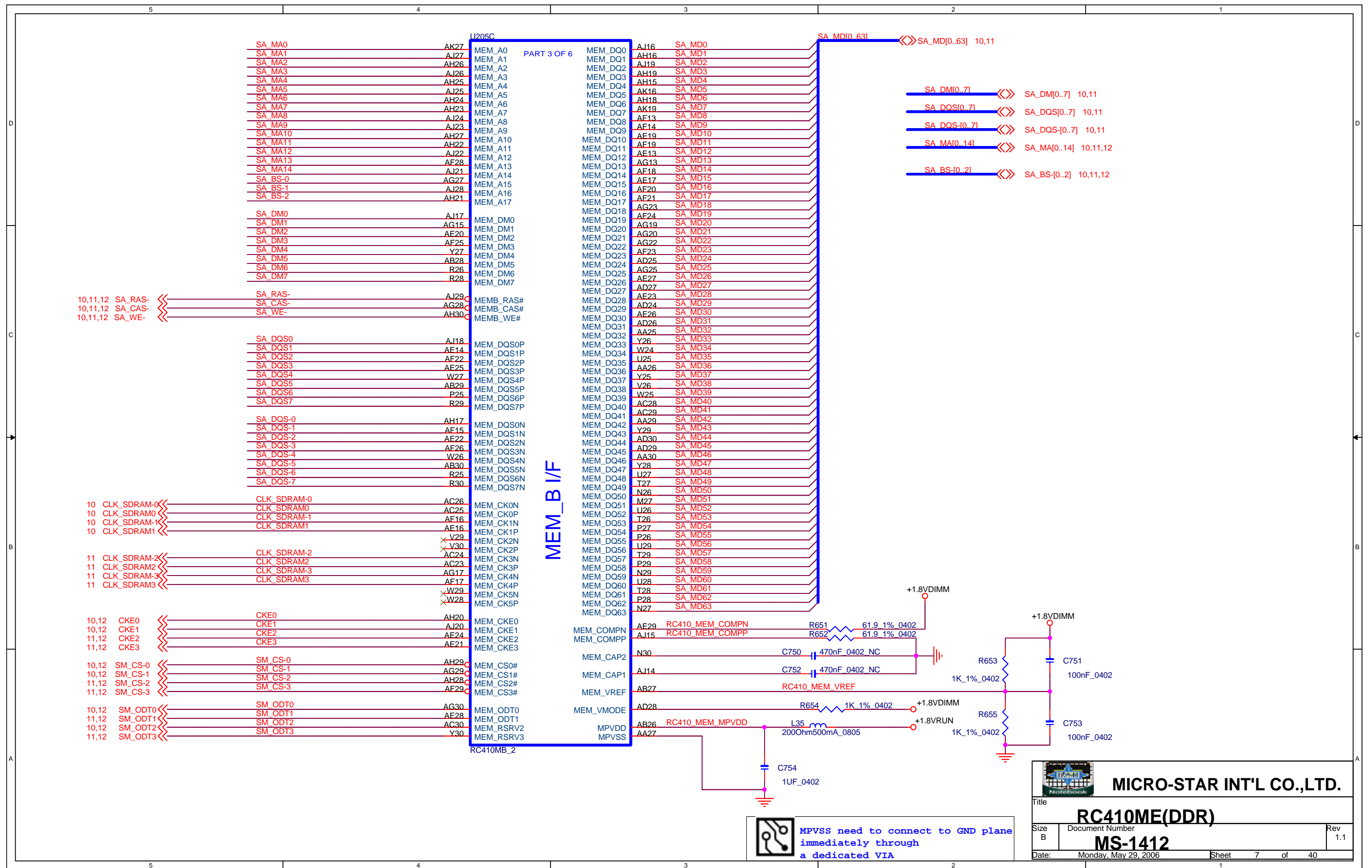
MICRO-STAR INT'L CO.,LTD.

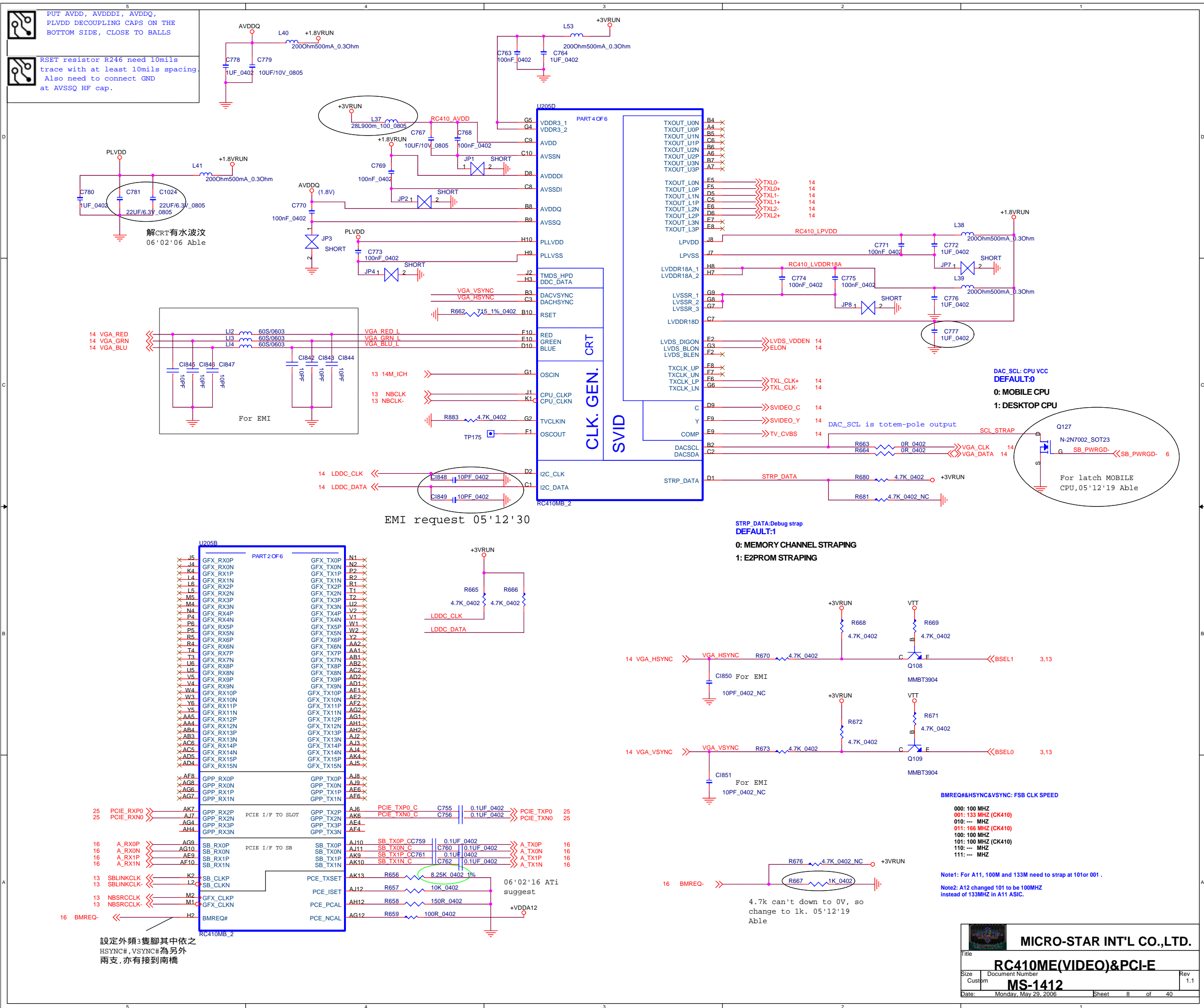
Title RC410ME(CPU)/PWRGD&FAN

Size Custom Document Number MS-1412

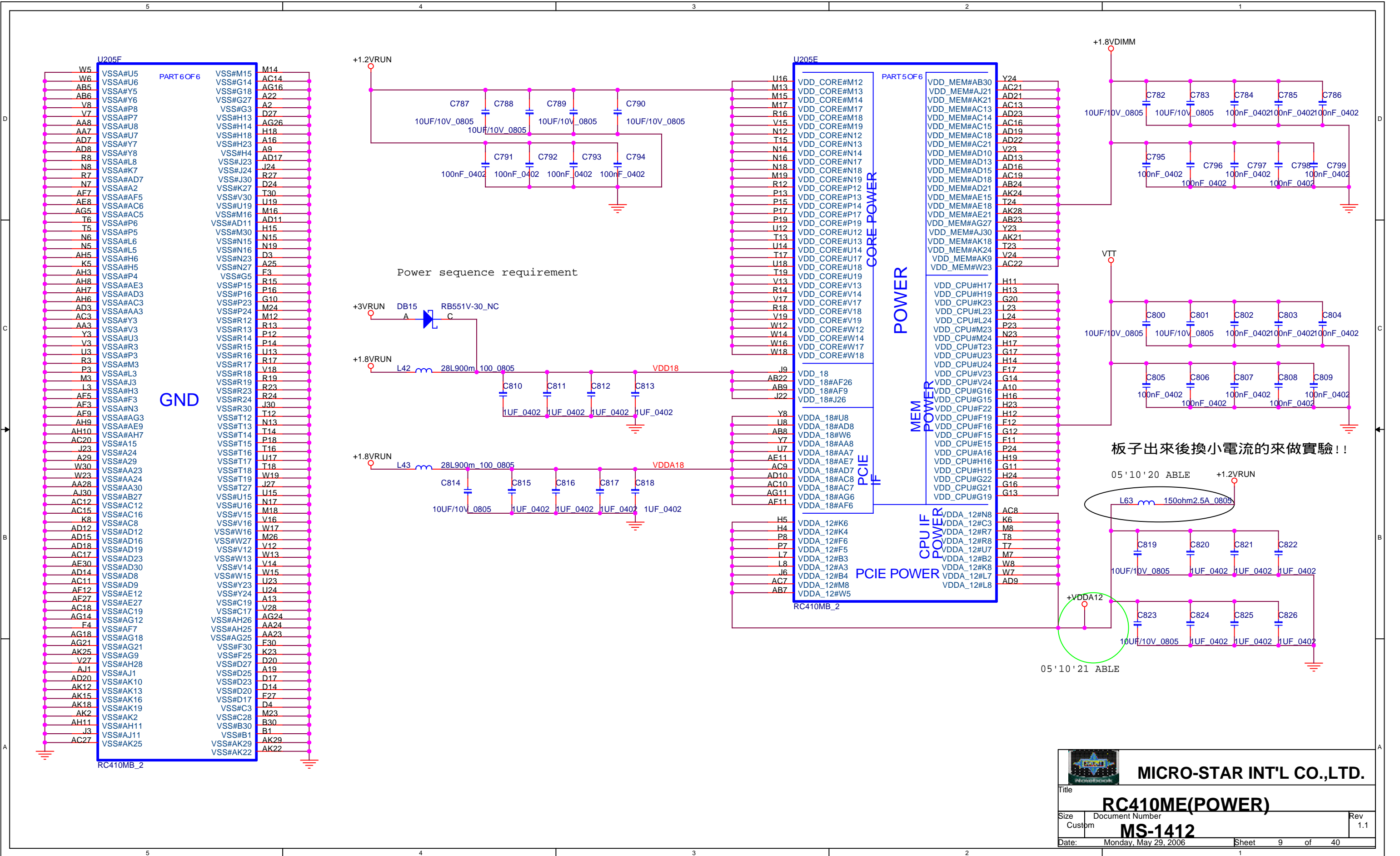
Date: Monday, May 29, 2006 Sheet 6 of 40

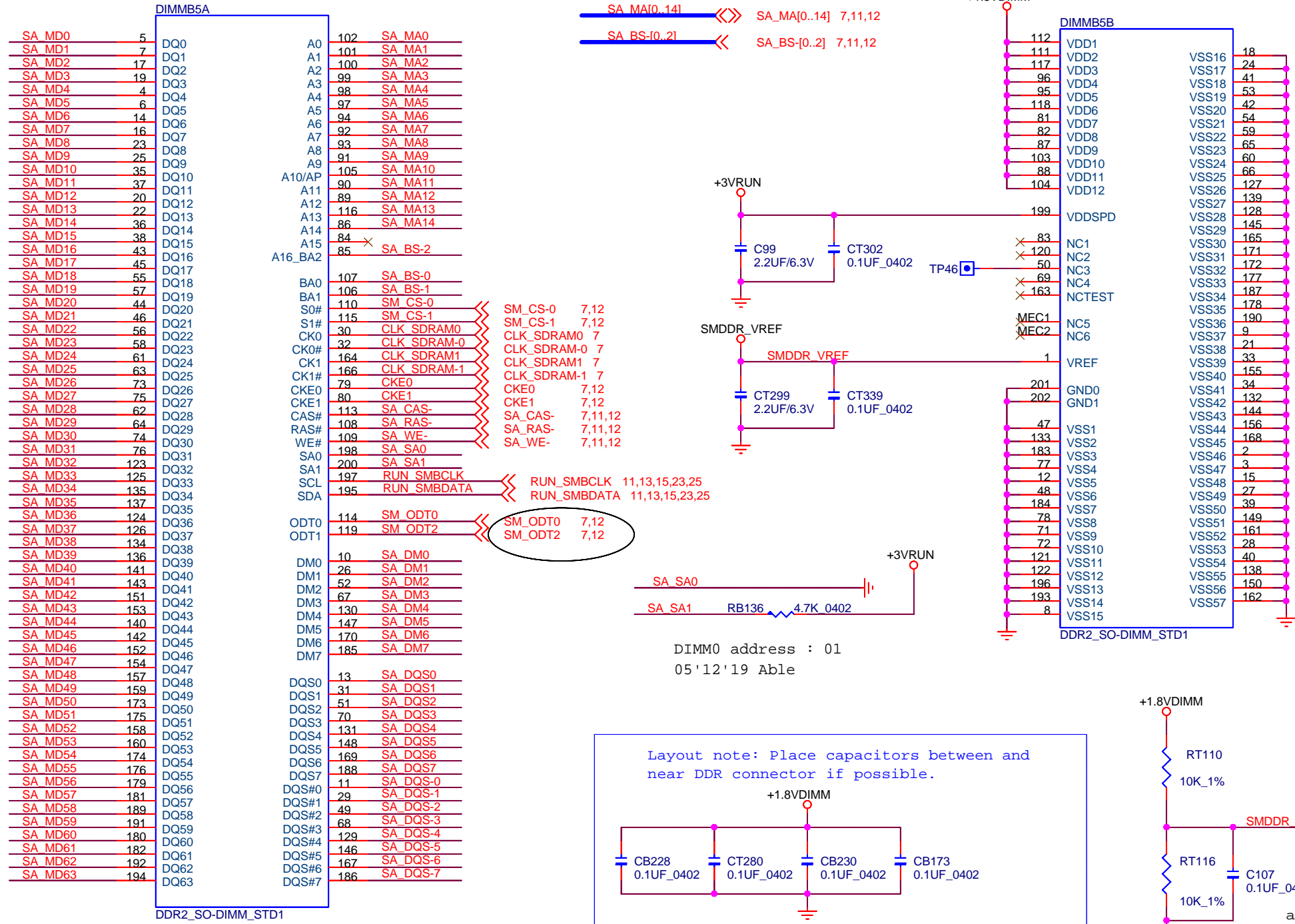













**MICRO-STAR INT'L CO.,LTD.**

**DDR2-SODIMM-0**

Size B

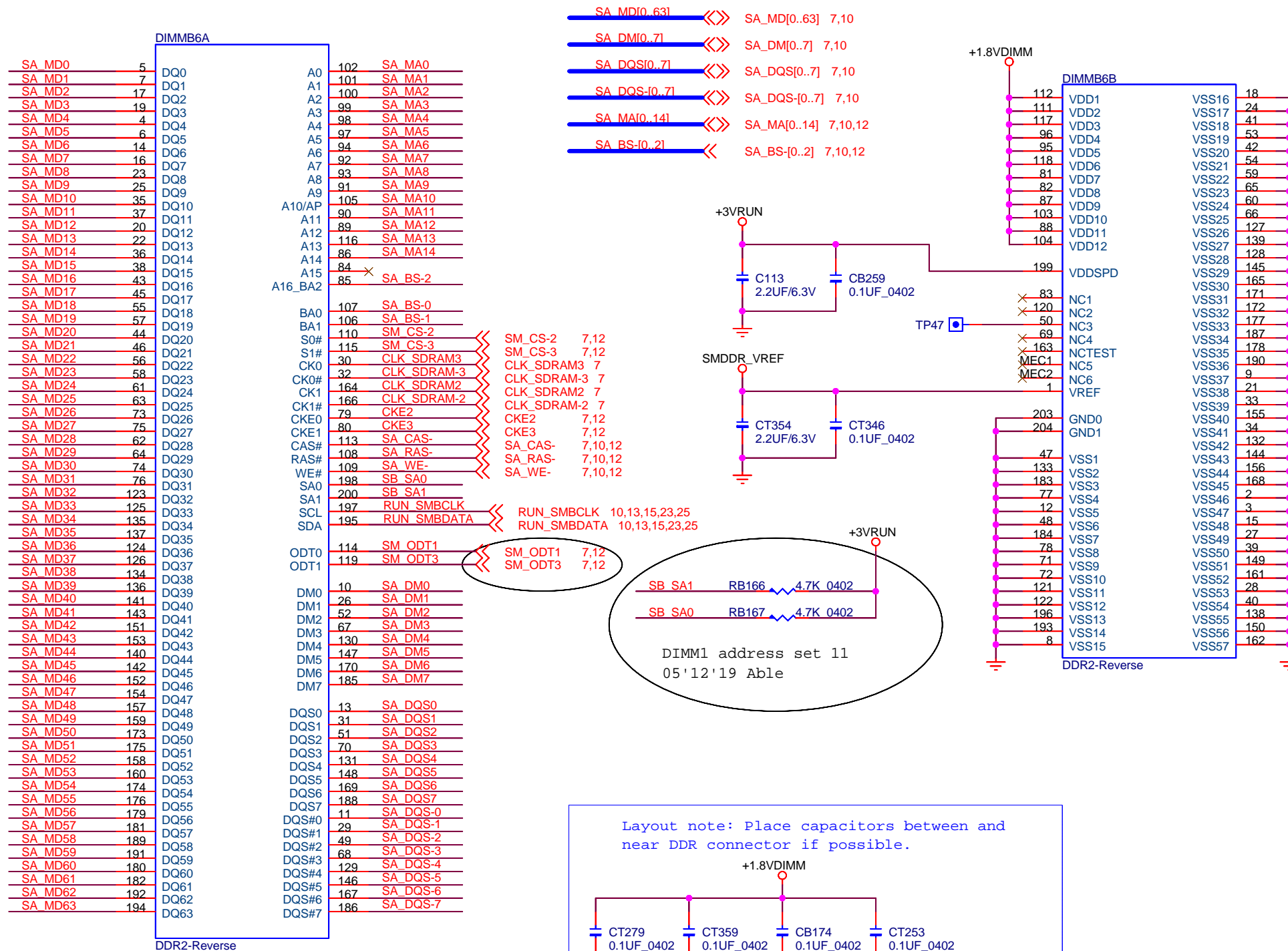
Document Number

**MS-1412**

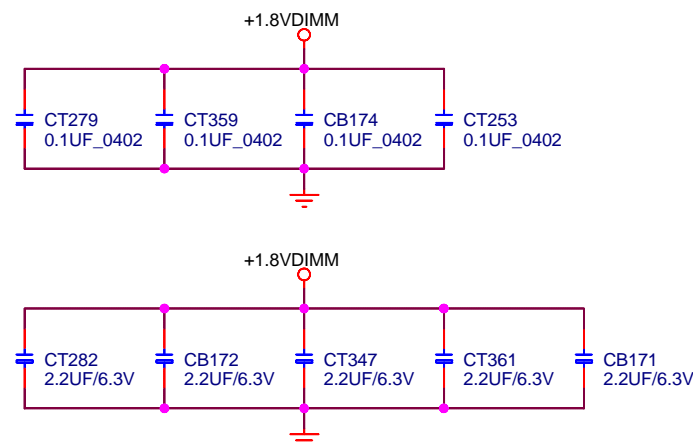
Date: Monday, May 29, 2006

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Rev 1.1



Layout note: Place capacitors between and near DDR connector if possible.



MICRO-STAR INT'L CO.,LTD.

Title

DDR2-SODIMM-1

Size  
B

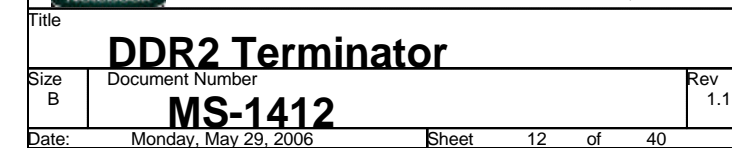
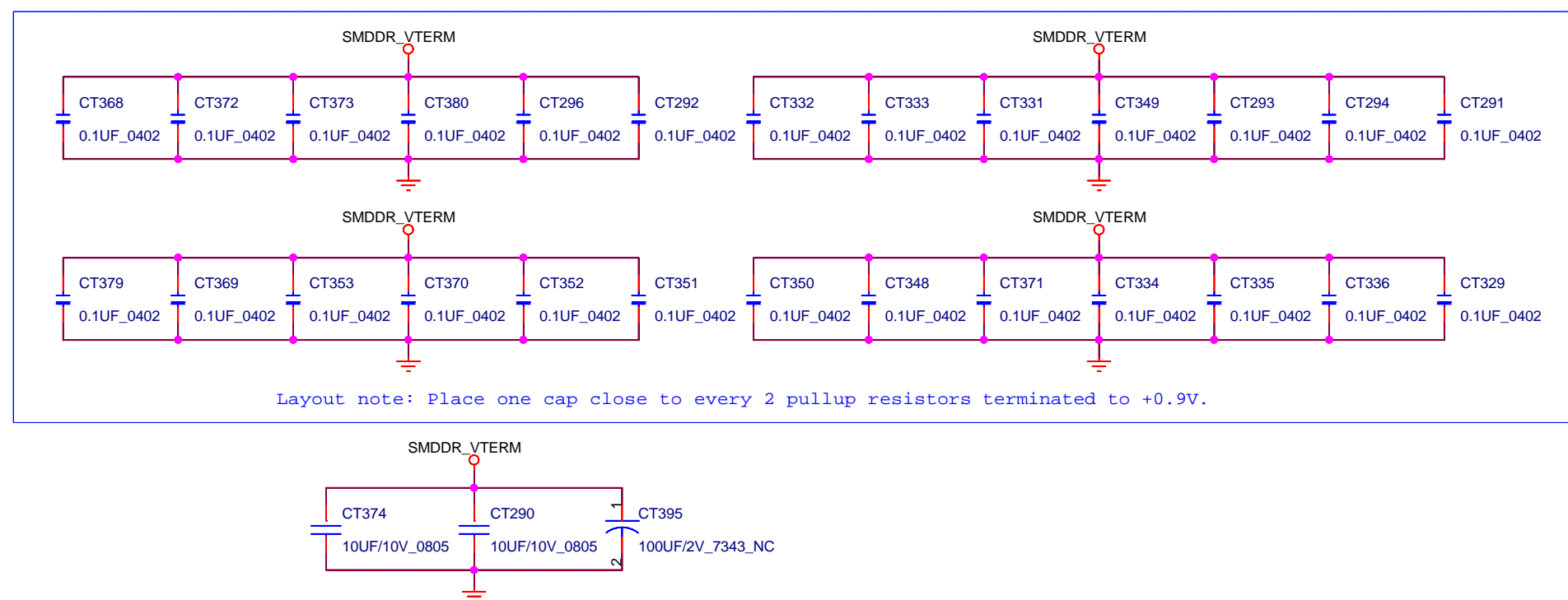
Document Number

MS-1412

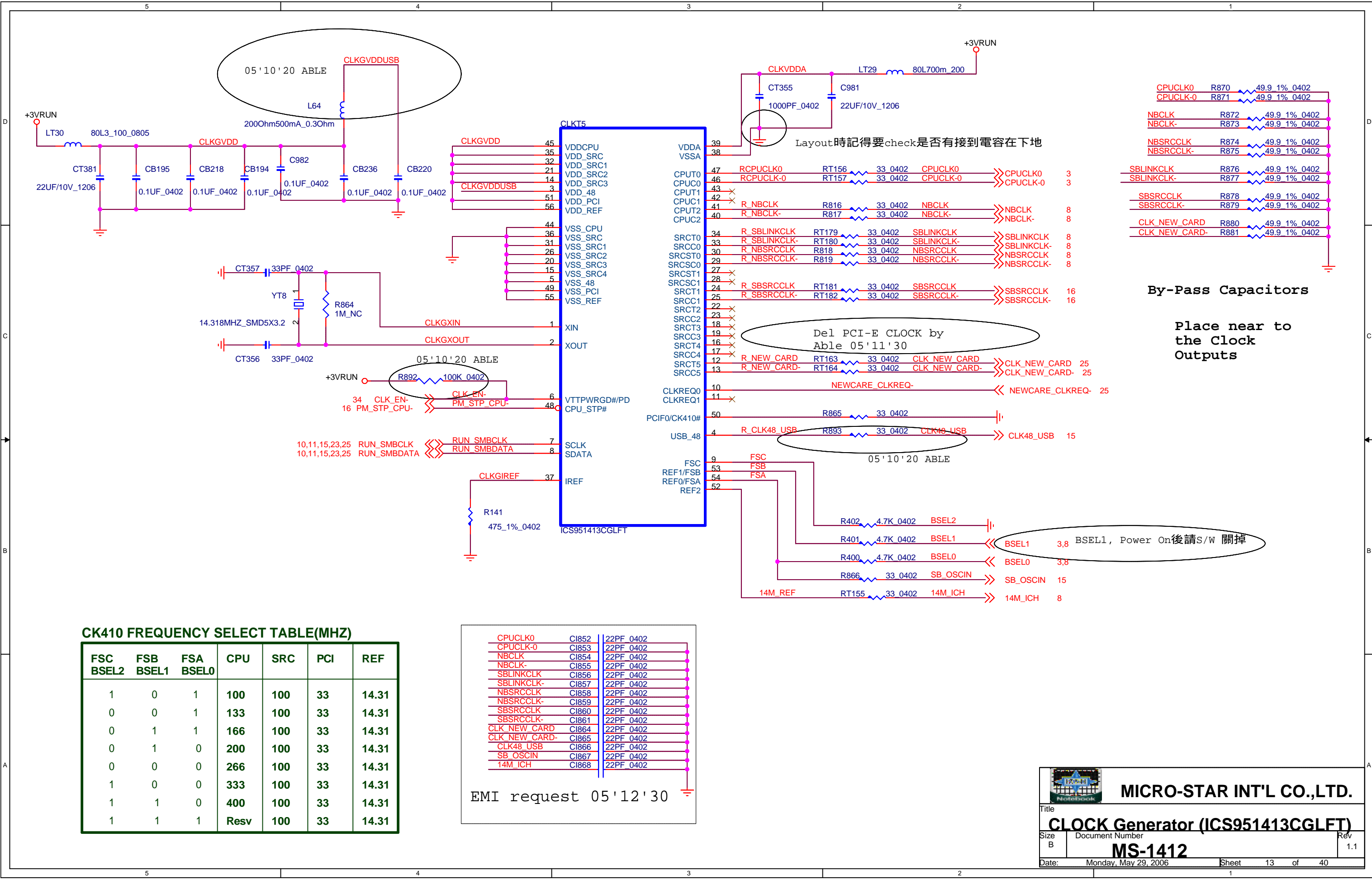
Rev  
1.1

Date: Monday, May 29, 2006

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CK410 FREQUENCY SELECT TABLE(MHZ)

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

CPUCLK0	CI852	22PF 0402
CPUCCLK-0	CI853	22PF 0402
NBCLK	CI854	22PF 0402
NBCLK-	CI855	22PF 0402
SBLINKCLK	CI856	22PF 0402
SBLINKCLK-	CI857	22PF 0402
NBSRCCLK	CI858	22PF 0402
NBSRCCLK-	CI859	22PF 0402
SBSRCCLK	CI860	22PF 0402
SBSRCCLK-	CI861	22PF 0402
CLK_NEW_CARD	CI864	22PF 0402
CLK_NEW_CARD-	CI865	22PF 0402
CLK48_USB	CI866	22PF 0402
SB_OSCIN	CI867	22PF 0402
14M_ICH	CI868	22PF 0402

EMI request 05'12'30

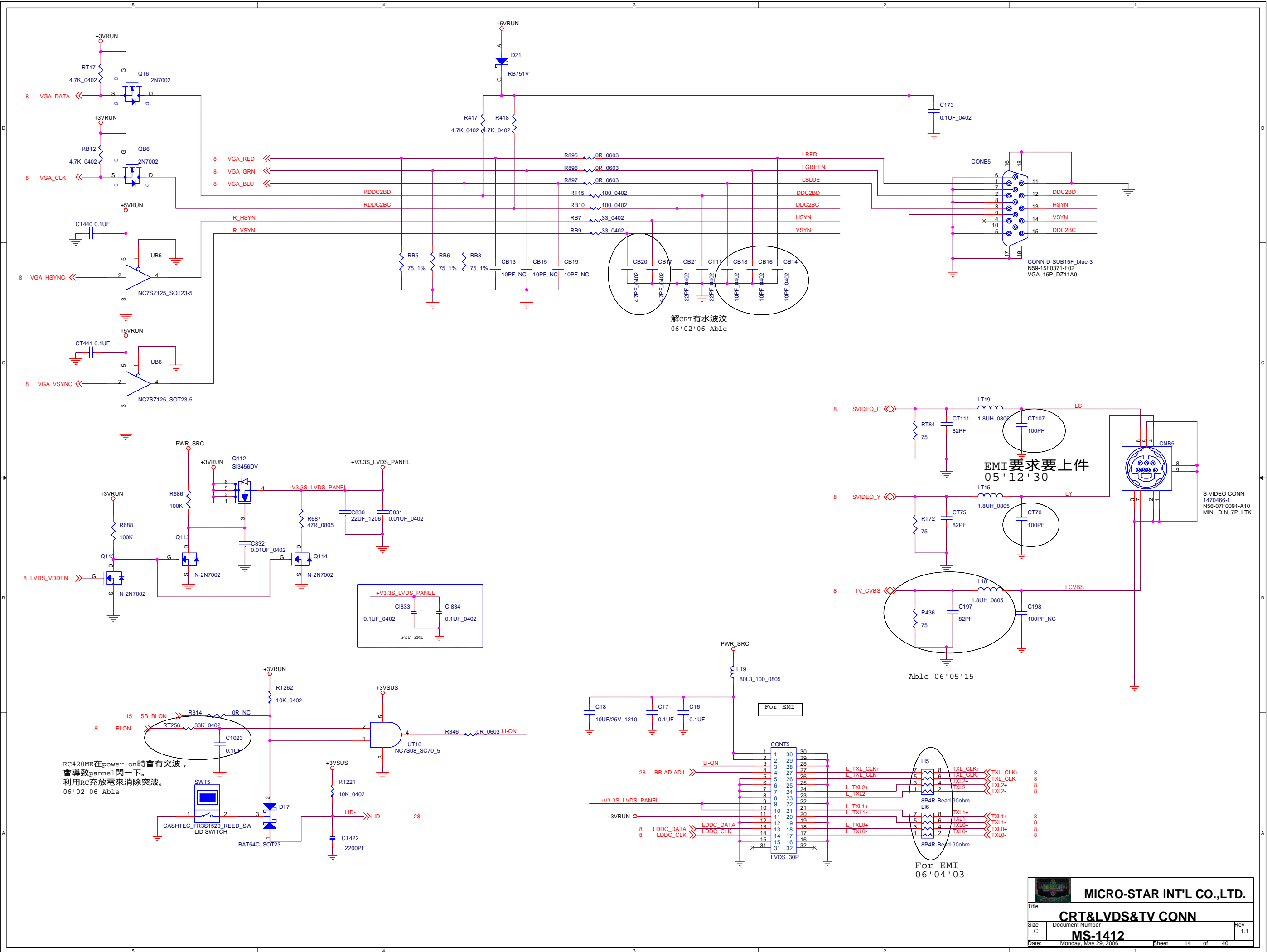
**MICRO-STAR INT'L CO.,LTD.**

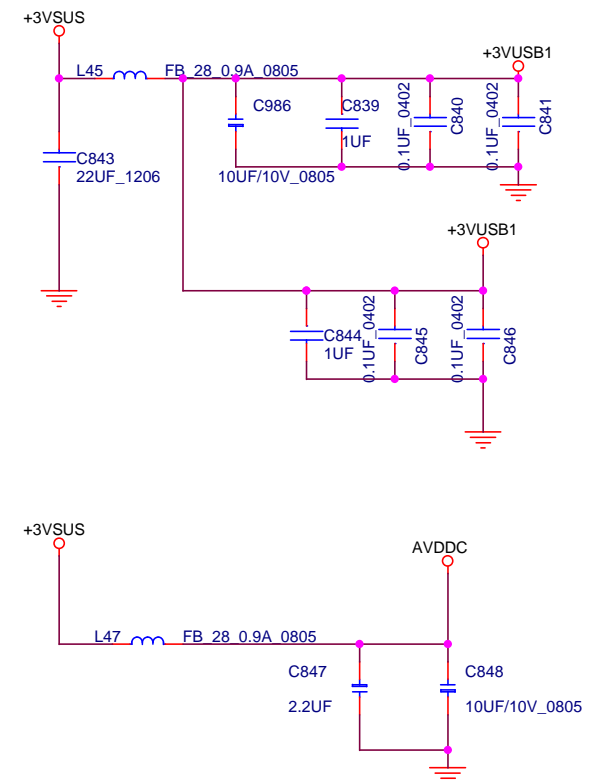
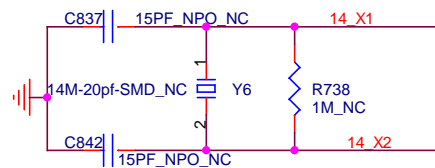
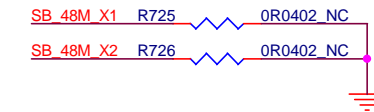
Title**CLOCK Generator (ICS951413CGLFT)**

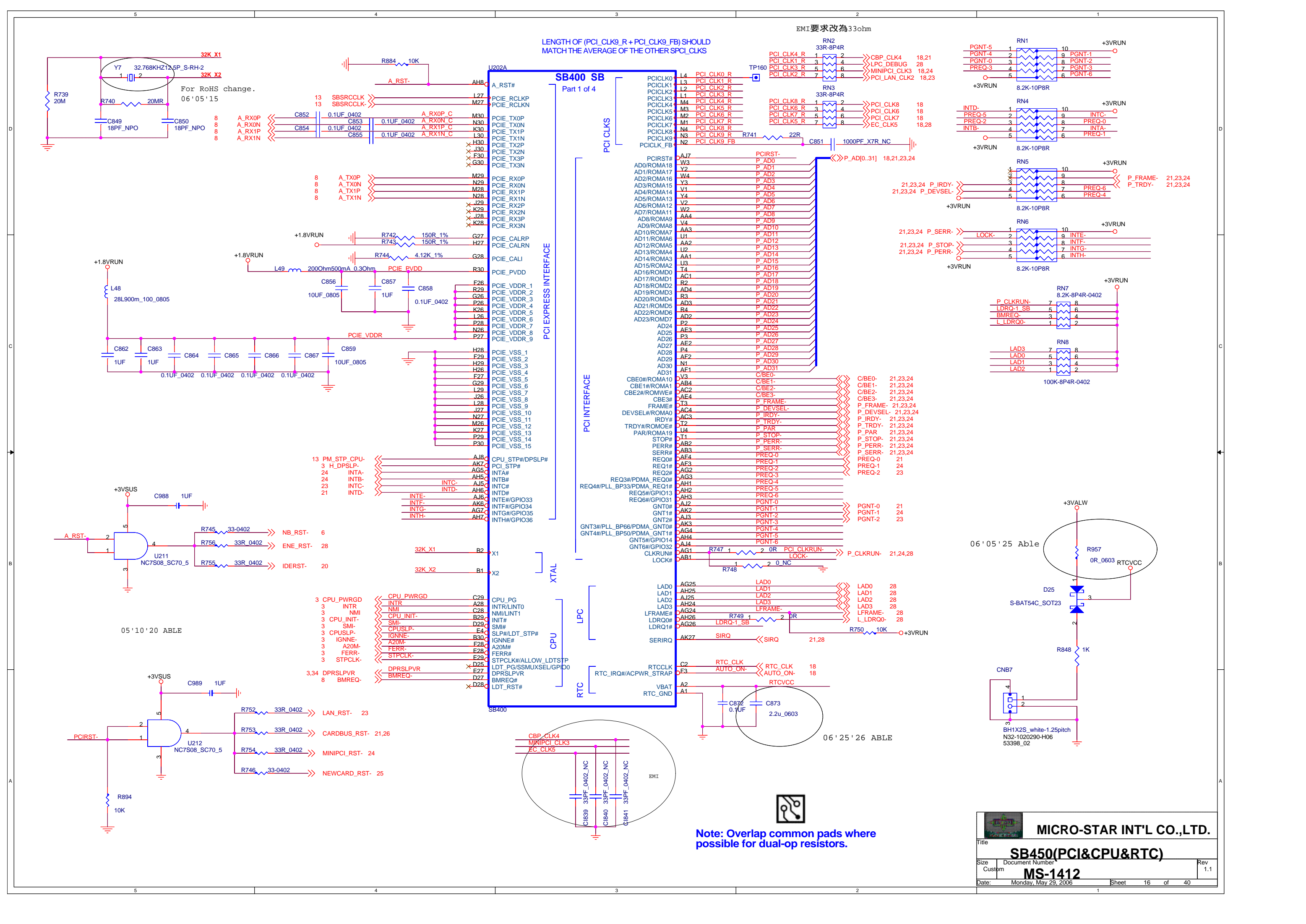
Size BDocument Number**MS-1412**Rev 1.1

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Note: Overlap common pads where possible for dual-op resistors.



MICRO-STAR INT'L CO.,LTD.

SB450(PCI&CPU&RTC)

MS-1412

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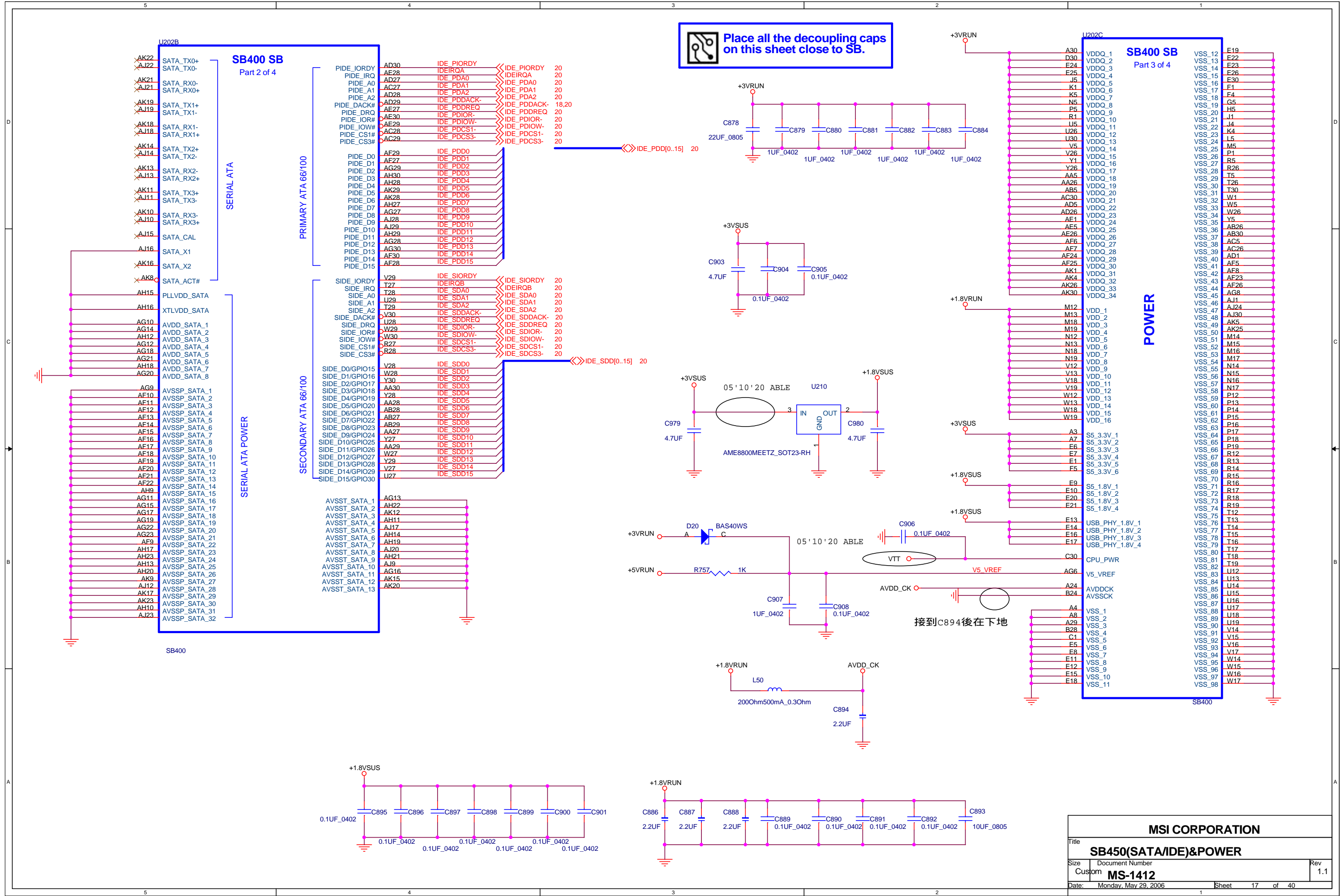
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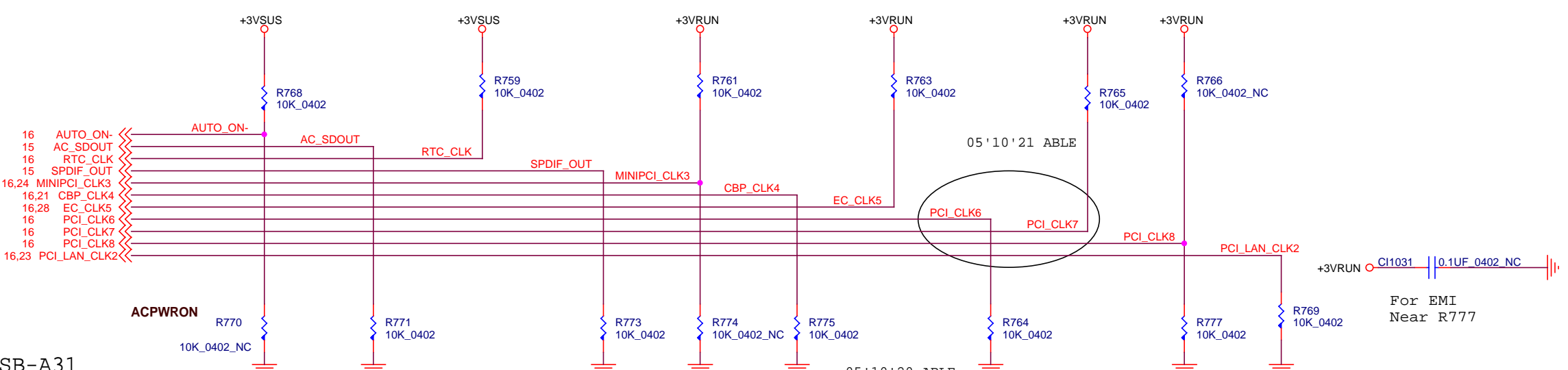
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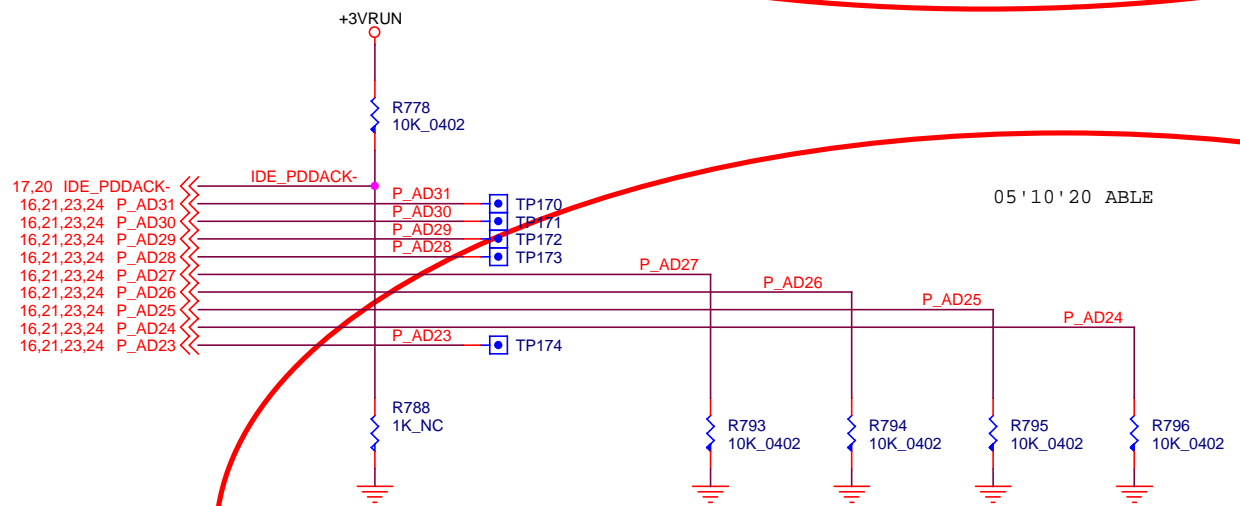




STRAP FOR SB-A31

Note: Overlap common pads where possible for dual-op resistors.

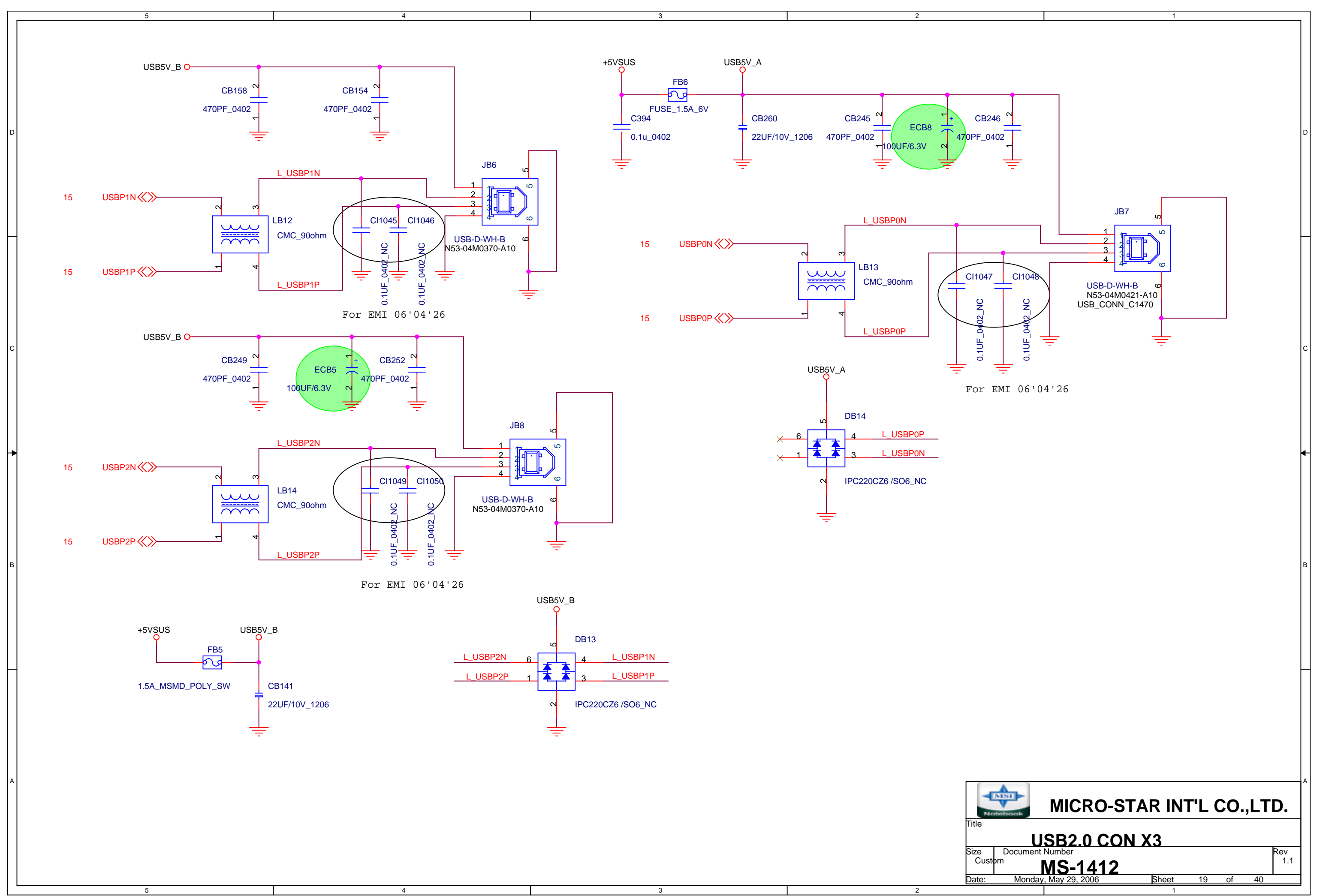
	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz XTAL MODE	USB PHY POWERDOWN DISABLE DEFAULT	Use internal PLL48	14MHZ OSC MODE DEFAULT	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM L, L = FWH ROM	DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	SIO 48MHz DEFAULT	48MHz OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE DEFAULT	Use external 48MHz clock DEFAULT	14MHZ XTAL MODE	CPU IF=P4 DEFAULT		



	P_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	RESERVED DEFAULT	RESERVED DEFAULT	RESERVED DEFAULT	RESERVED DEFAULT	BYPASS internal PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	USE USB PLL
PULL LOW	USE SHORT RESET					USE internal PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BYPASS USB PLL

LONG RESET -->A21







16,18,23,24 P\_AD[0..31] << P\_AD[0..31]

P_AD31	F5	AD31
P_AD30	F4	AD30
P_AD29	G7	AD29
P_AD28	G5	AD28
P_AD27	G4	AD27
P_AD26	H7	AD26
P_AD25	H6	AD25
P_AD24	H5	AD24
P_AD23	J5	AD23
P_AD22	J4	AD22
P_AD21	K5	AD21
P_AD20	K6	AD20
P_AD19	L6	AD19
P_AD18	L7	AD18
P_AD17	M4	AD17
P_AD16	M5	AD16
P_AD15	T5	AD15
P_AD14	R6	AD14
P_AD13	T6	AD13
P_AD12	N7	AD12
P_AD11	R7	AD11
P_AD10	N8	AD10
P_AD9	P8	AD9
P_AD8	R8	AD8
P_AD7	N9	AD7
P_AD6	R9	AD6
P_AD5	T9	AD5
P_AD4	R10	AD4
P_AD3	T10	AD3
P_AD2	P10	AD2
P_AD1	N10	AD1
P_AD0	T11	AD0

16,23,24 C/BE3- << C/BE3-  
16,23,24 C/BE2- << C/BE2-  
16,23,24 C/BE1- << C/BE1-  
16,23,24 C/BE0- << C/BE0-

16,18 CBP\_CLK4 << CBP\_CLK4  
16,23,24 P\_DEVSEL- << P\_DEVSEL-  
16,23,24 P\_FRAME- << P\_FRAME-  
16,23,24 P\_IRDY- << P\_IRDY-  
16,23,24 P\_TRDY- << P\_TRDY-  
16,23,24 P\_STOP- << P\_STOP-  
16,23,24 P\_PAR- << P\_PAR-  
16,23,24 P\_PERR- << P\_PERR-  
16,23,24 P\_SERR- << P\_SERR-  
16 PREQ-0 << PREQ-0  
16 PGNT-0 << PGNT-0  
16,26 CARDBUS\_RST- << CARDBUS\_RST-

15,23,24 P\_PME- << P\_PME-

26 PCMSPK << PCMSPK

16,24,28 P\_CLKRUN- << P\_CLKRUN-  
22 MS\_CD- << MS\_CD-  
16,28 SIRQ << SIRQ  
16 INTD- << INTD-

PCMSPK R855 100K\_NC  
PCMSPK R856 100K

C/BE3#  
C/BE2#  
C/BE1#  
C/BE0#

IDSEL  
PCI\_CLK  
DEVSEL#  
FRAME#  
IRDY#  
TRDY#  
STOP#  
PAR  
PERR#  
SERR#  
REQ#  
GNT#  
RST#

RI\_OUT/PME#

SPKR\_OUT#  
SKTA\_LEDON  
ODR\_LEDON

MF6/CLKRUN#  
MF4/MS\_CD#  
MF3  
MF0

O2\_OZ711MP1

OZ711MP

1394

TEST\_PHY

VR\_CPR0  
VR\_CPR1

NC0  
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NC2  
NC3

CAVCC

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C299 X\_0.1UF\_0402

C299 X\_0.1UF\_0402

C299 X\_0.1UF\_0402

C299 X\_0.1UF\_0402

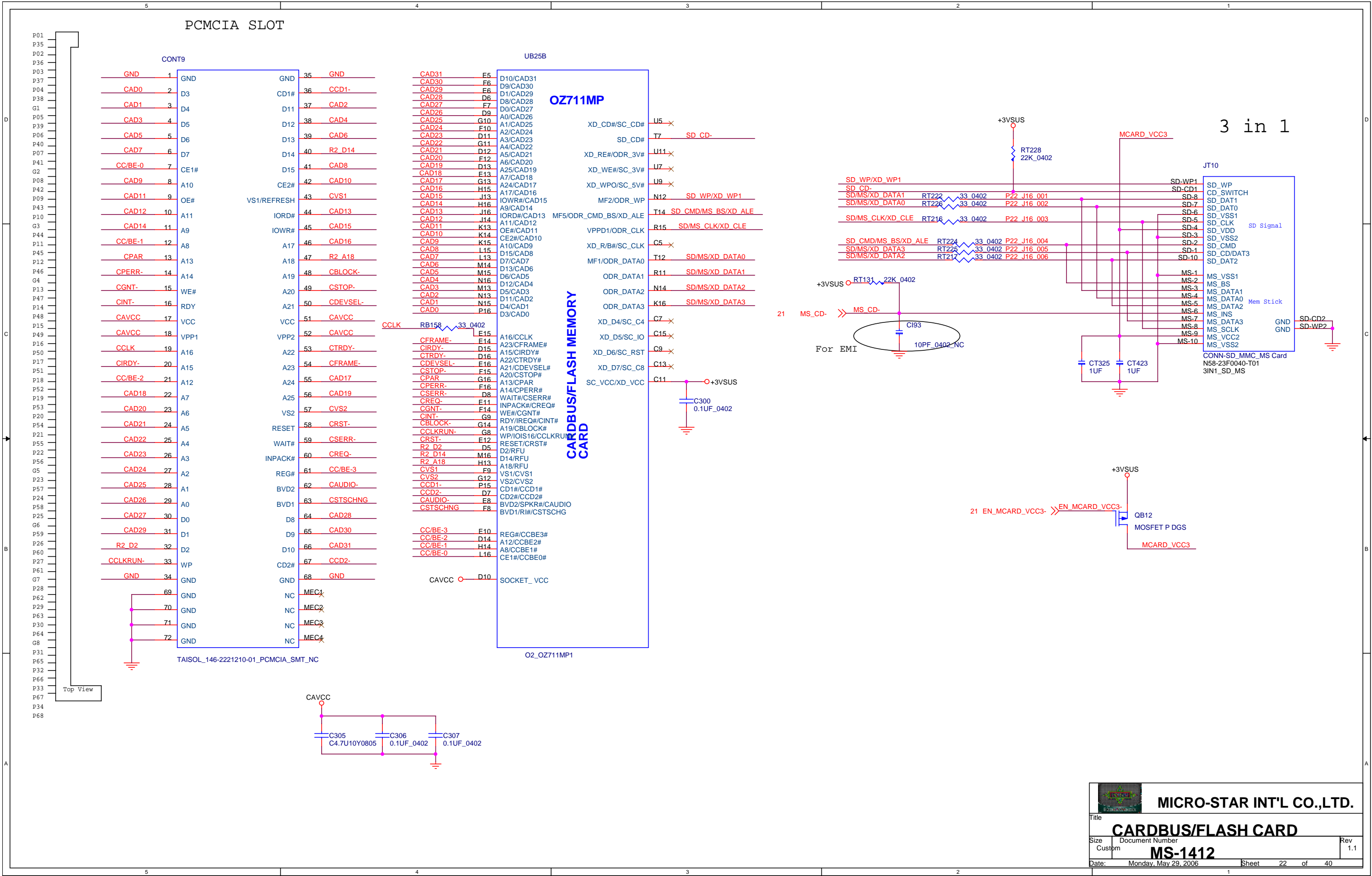
C299 X\_0.1UF\_0402

C299 X\_0.1UF\_0402

C299 X\_0.1UF\_0402

C299 X\_0.1UF\_0402

C299 X\_0.1UF\_0402



	DVDD	DVDDA	AVDDL	AVDDH	V-12P
8100C	2.5V	2.5V	3.3V	X	2.5V
8110S	1.8V	1.8V	2.5V	3.3V	X
8110SB	1.2V	1.2V	2.5V	3.3V	3.3V

The image displays three PCB layout diagrams for the LAN section of the T1000 module.

**Top Diagram:** Shows the power plane layout for the LAN section. It includes decoupling capacitors (C992, C993, C994, C995, C996, C997, C998, C999, C1000) and inductors (L65, L66, L67) connected to various power pins (CTRL18, CTRL25, VDD33, DVDD, V<sub>12P</sub>, AVDDL, AVDDH). The layout also shows the placement of capacitors C991, C992, C993, C994, C995, C996, C997, C998, C999, and C1000.

**Bottom Diagram:** Shows the power plane layout for the LAN section, including decoupling capacitors (C1004, C1005, C1006, C1007, C1008, C1009, C1010) and inductors (L66, L67) connected to various power pins (CTRL25, VDD33, AVDDL, AVDDH, V<sub>12P</sub>). The layout also shows the placement of capacitors C1004, C1005, C1006, C1007, C1008, C1009, and C1010.

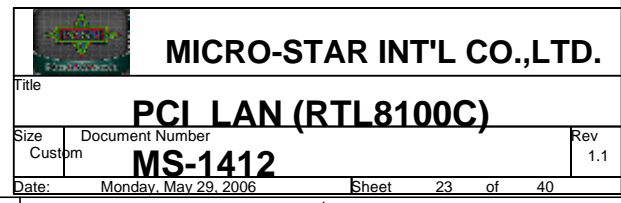
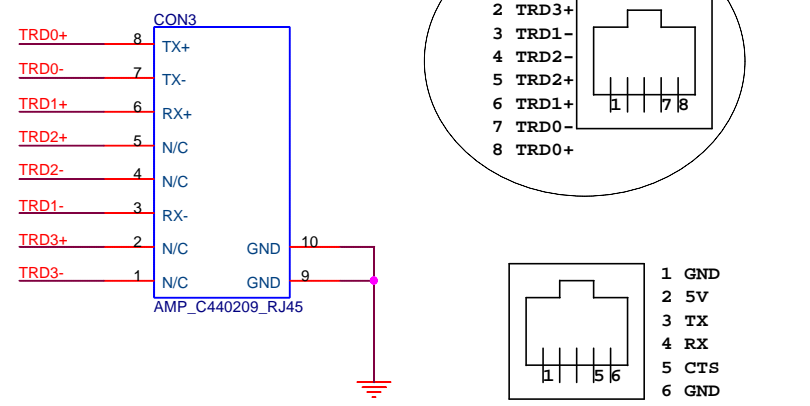
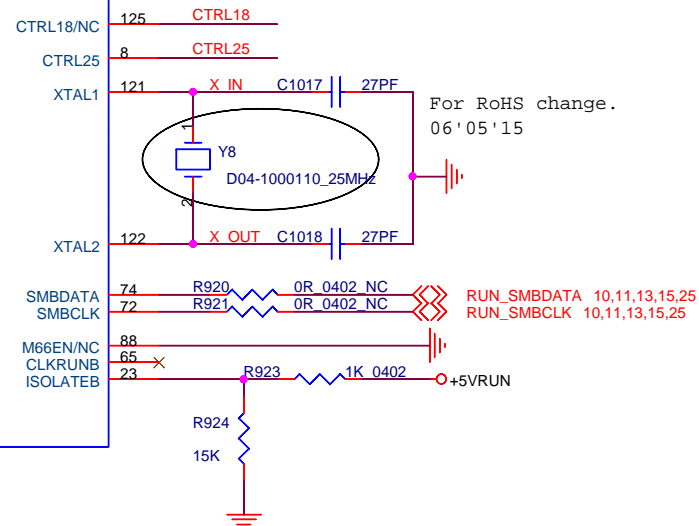
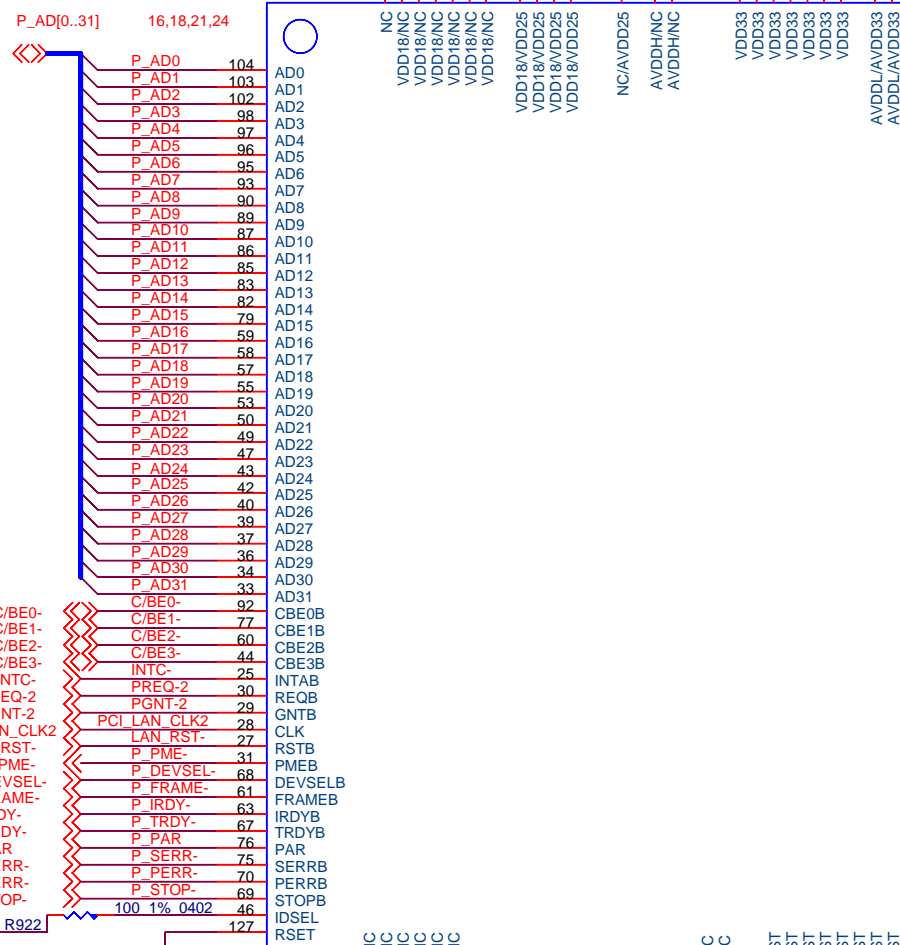
**Right Diagram:** Shows the LAN chip connection. It includes a table of pin connections and a note about the placement of capacitors.

Pin	Component	Value	Notes
MDIO+	R904	75 1% 0402	
MDIO-	R906	75 1% 0402	
MDI1+	R907	75 1% 0402	
MDI1-	R909	75 1% 0402	
MDI2+	R912	49.9 1% 0402	NC
MDI2-	R914	49.9 1% 0402	NC
MDI3+	R915	49.9 1% 0402	NC
MDI3-	R917	49.9 1% 0402	NC

Place at pin 26, 41, 56, 71, 84, 94, 107

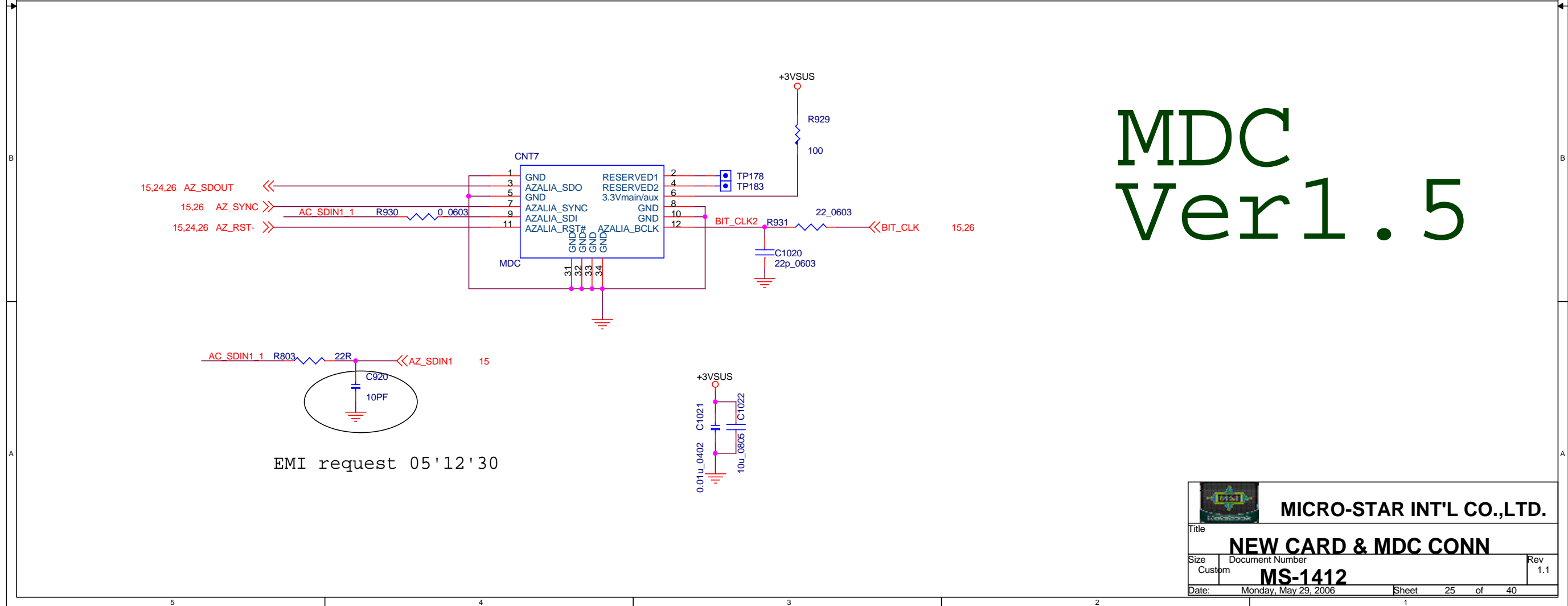
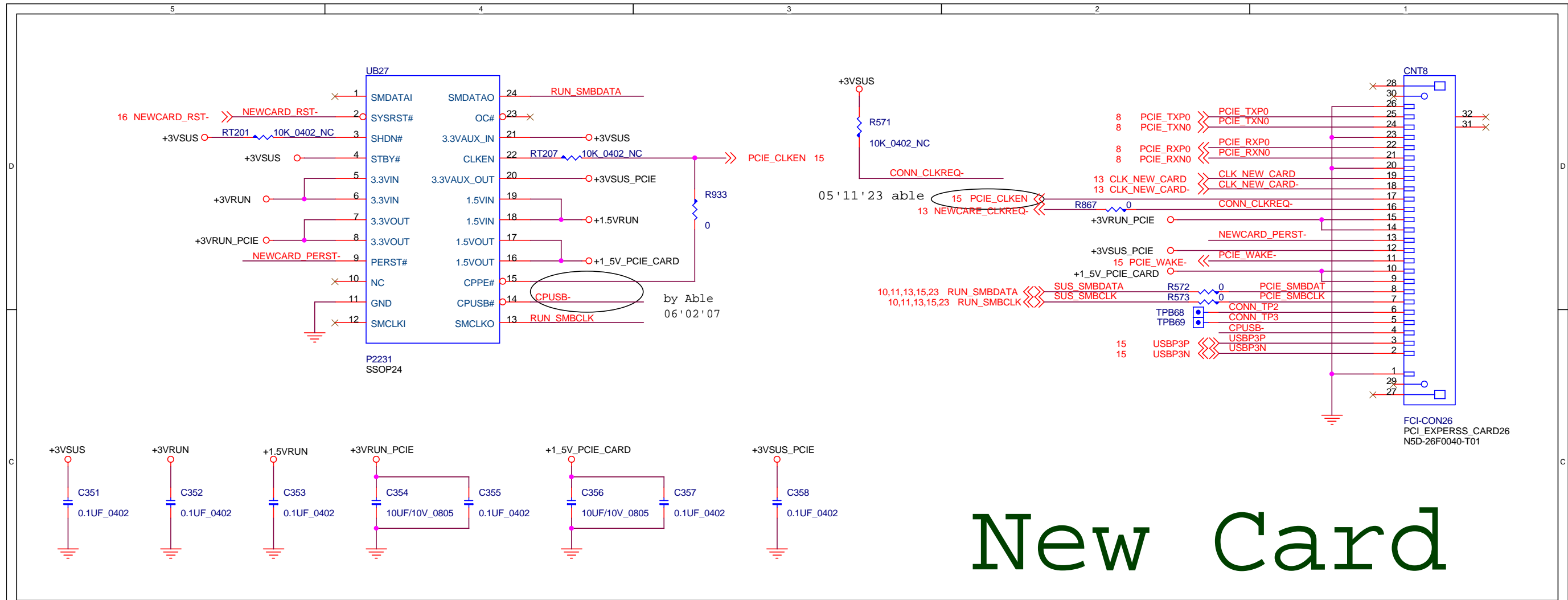
Place at pin 10, 120

Close to LAN Chip. 8100C use 0.1u; 8110SX use 0.01u

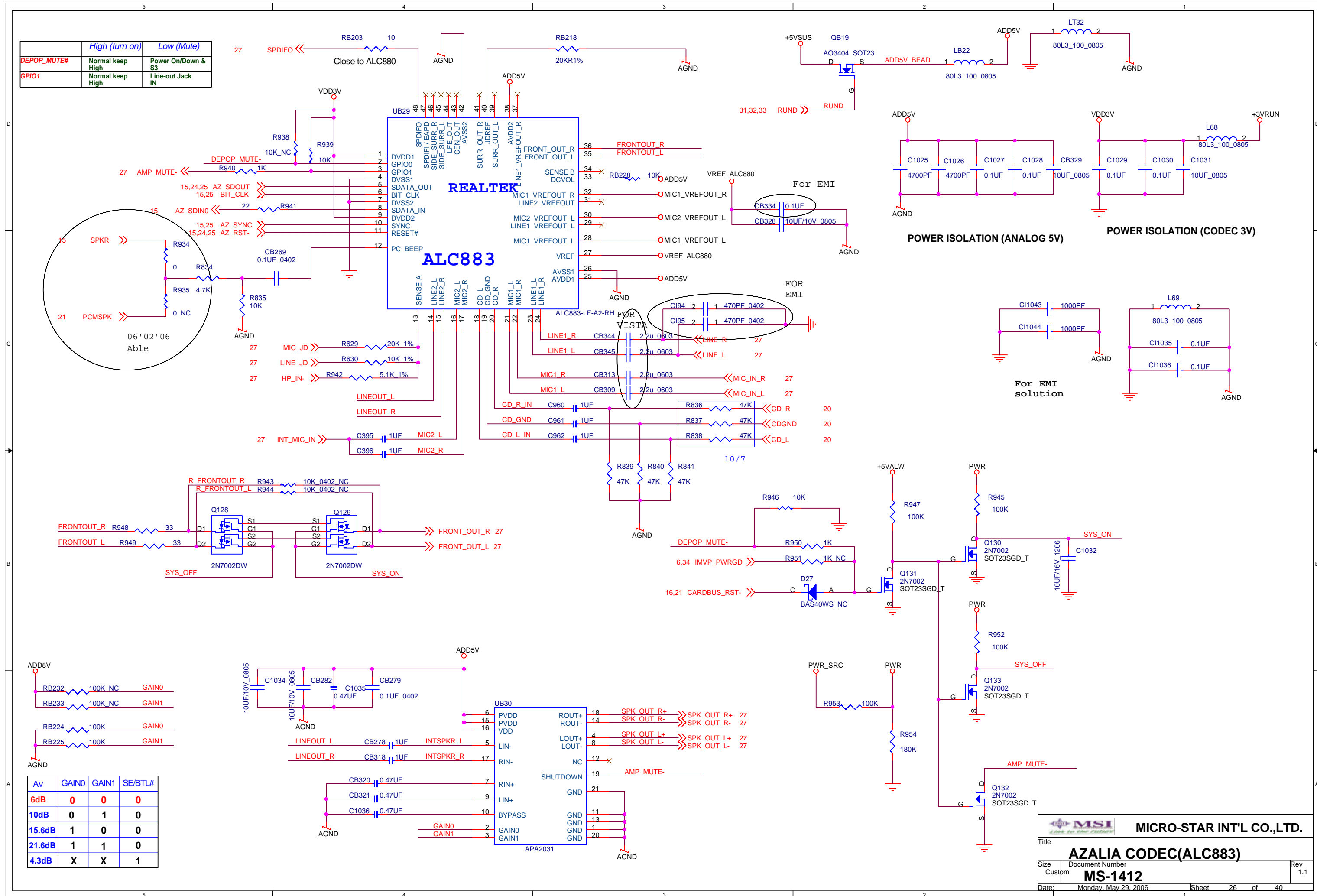




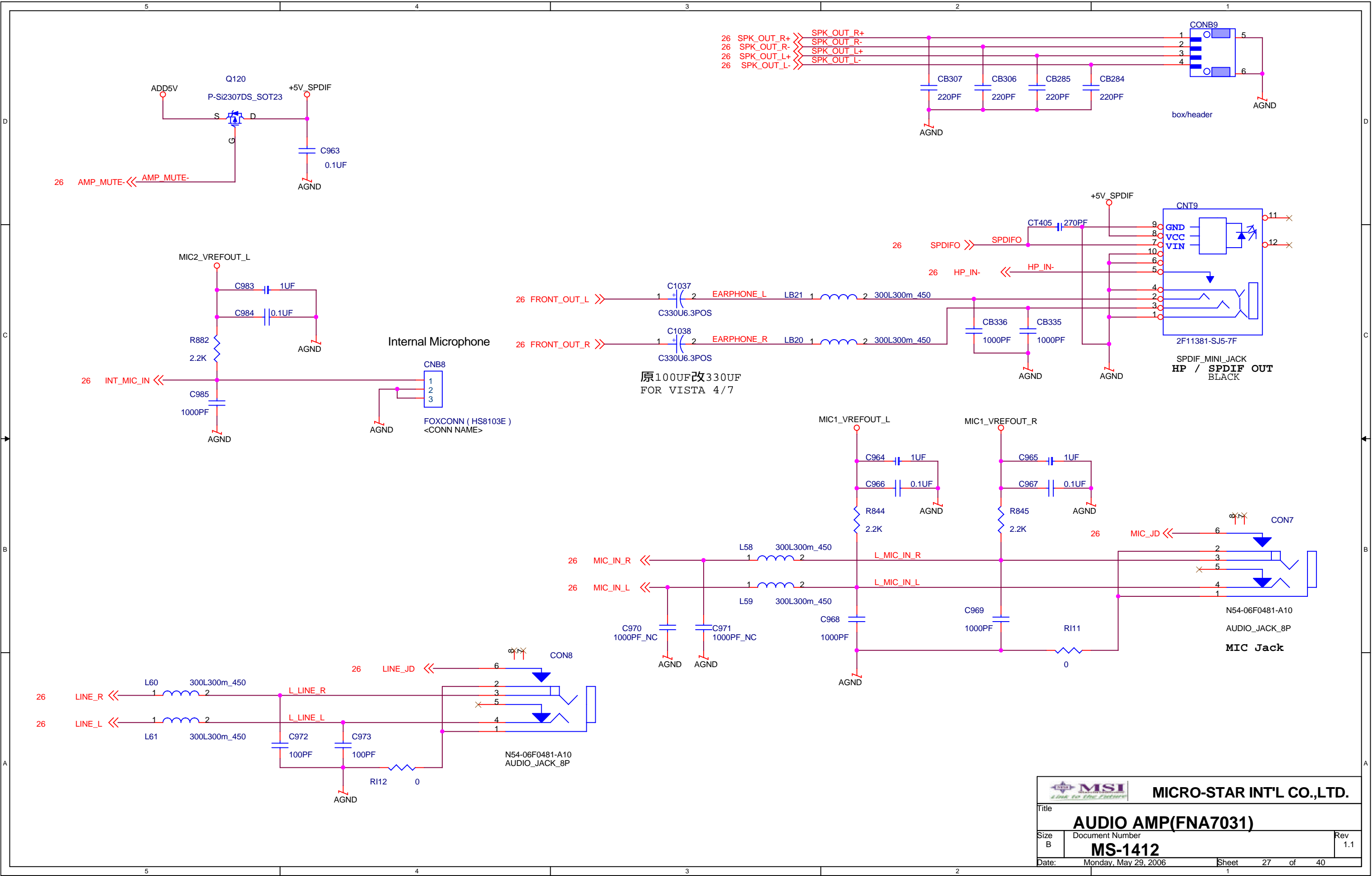




	<i>High (turn on)</i>	<i>Low (Mute)</i>
<b>DEPOP_MUTE#</b>	Normal keep High	Power On/Down & S3
<b>GPIO1</b>	Normal keep High	Line-out Jack IN

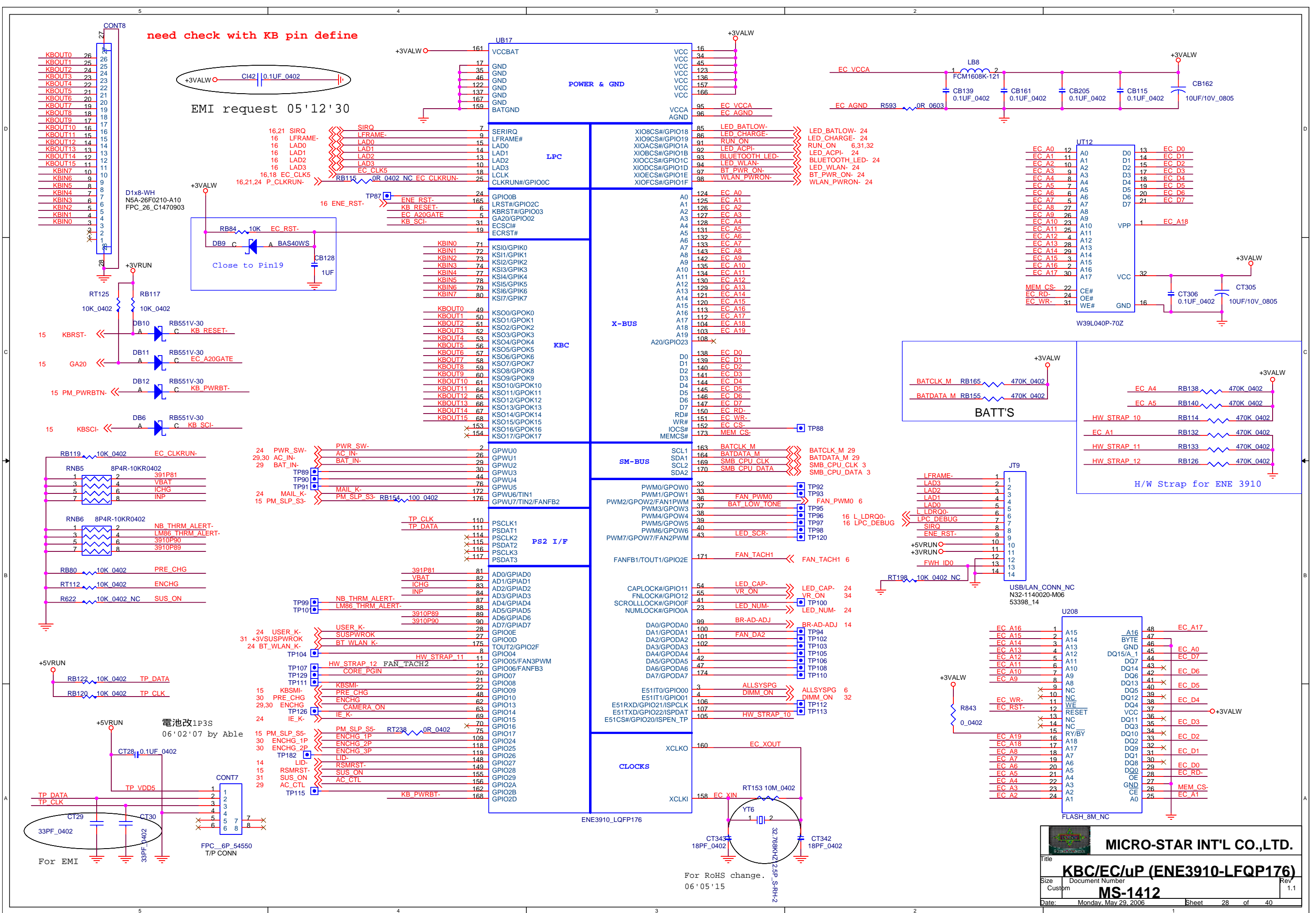


Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1

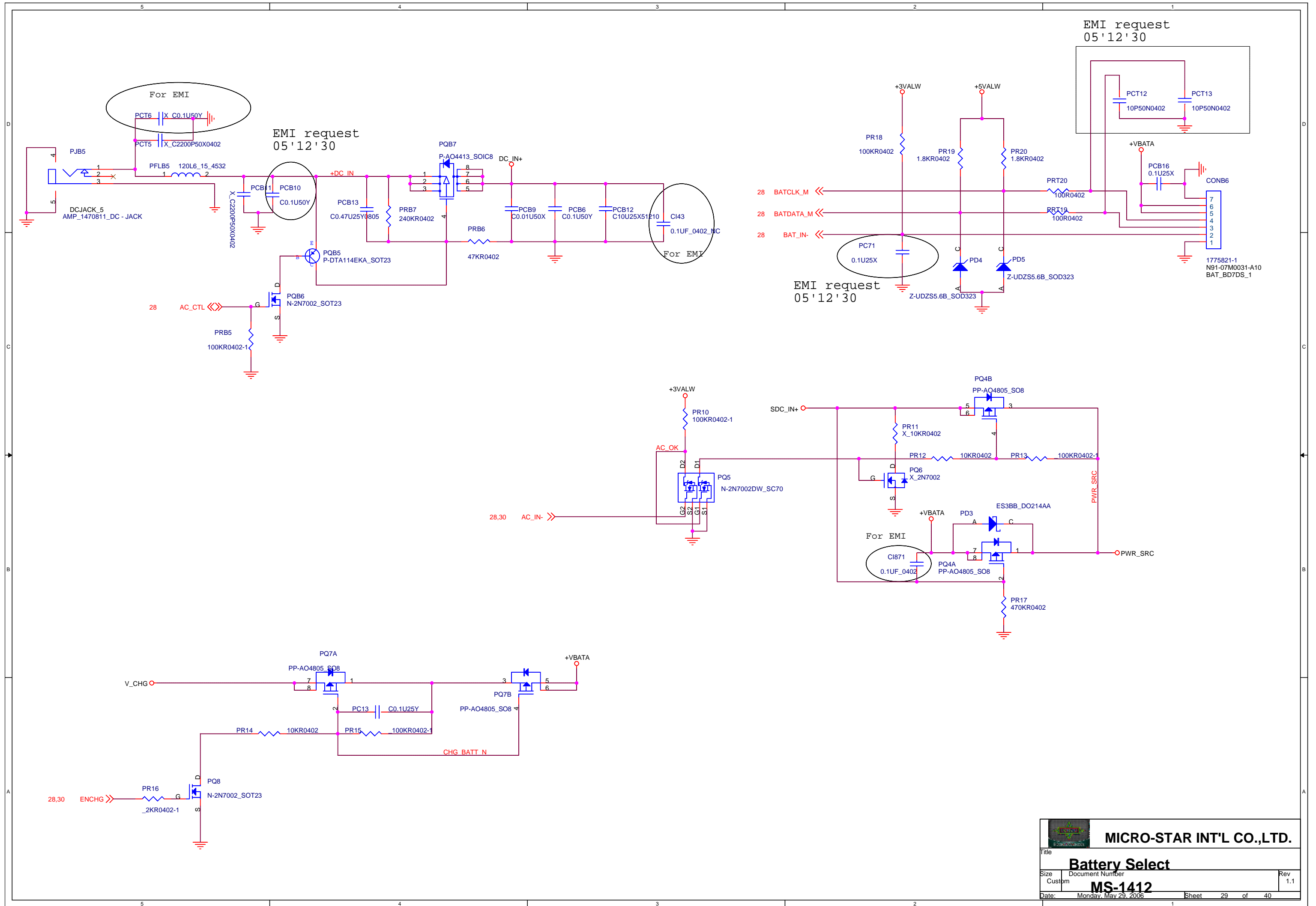


need check with KB pin define

EMI request 05'12'30

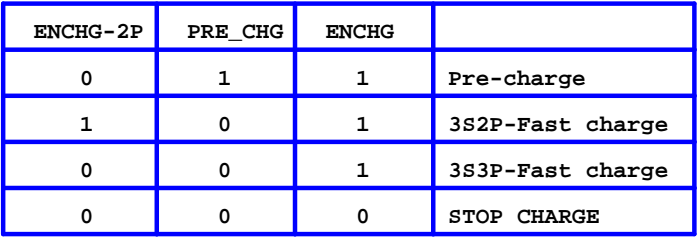






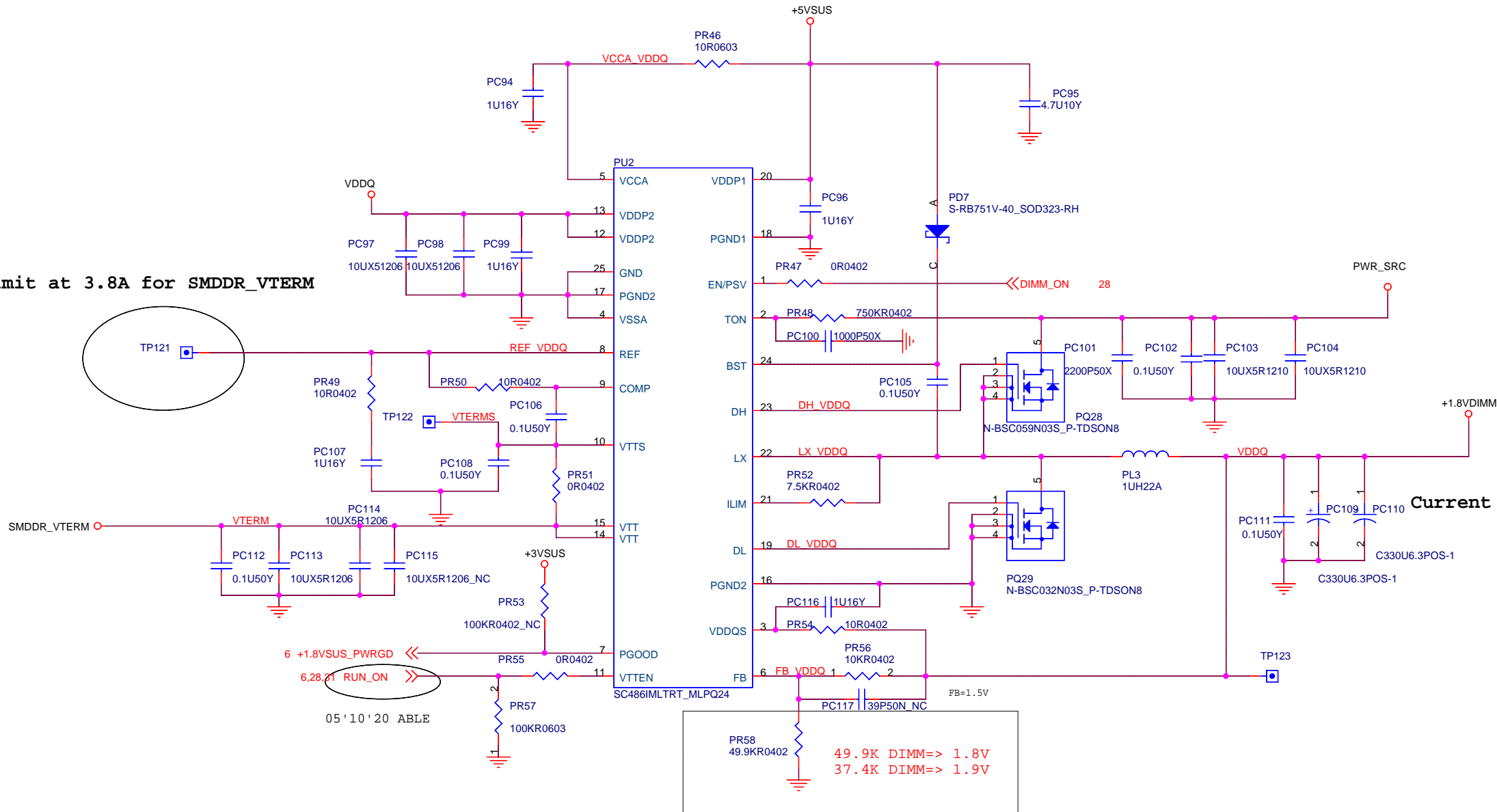
MICRO-STAR INT'L CO.,LTD.

Title		Battery Select	
Size	Custom	Document Number	Rev
MS-1412			1.1
Date: Monday, May 29, 2006		Sheet	29 of 40



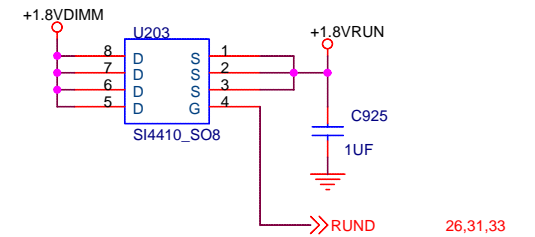


Current limit at 3.8A for SMDDR\_VTERM



Current limit at 15A for +1.8VSUS

Current limit at 3.38A for +1.8VVRUN



For EMI

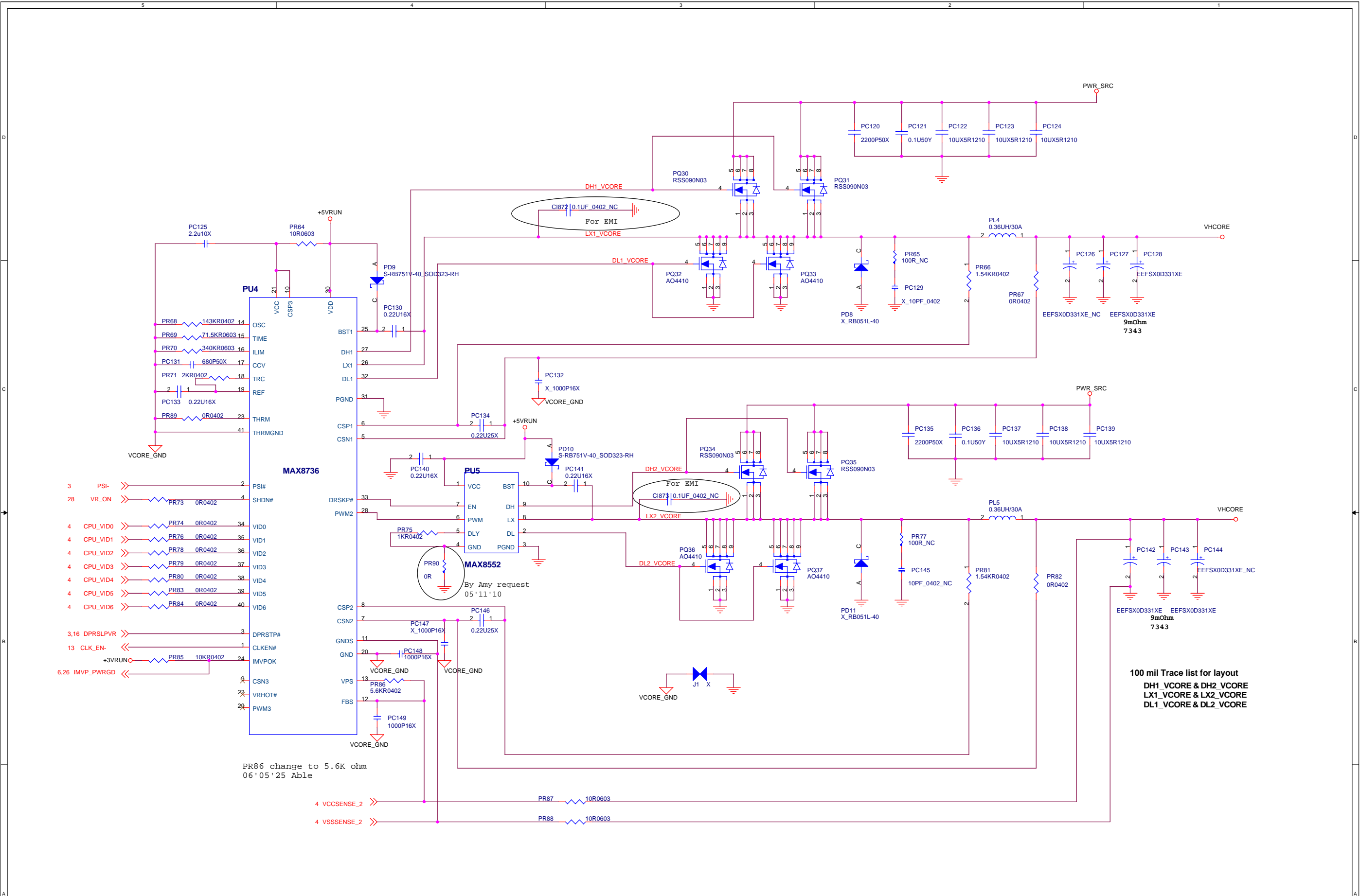
Title		
M_VDDR & +1.8VDIMM		
Size	Document Number	Rev
Custom	MS-1412	1.1
Date:	Monday, May 29, 2006	Sheet 32 of 40

The Limited Current =6A

Current Limit at 12Amp

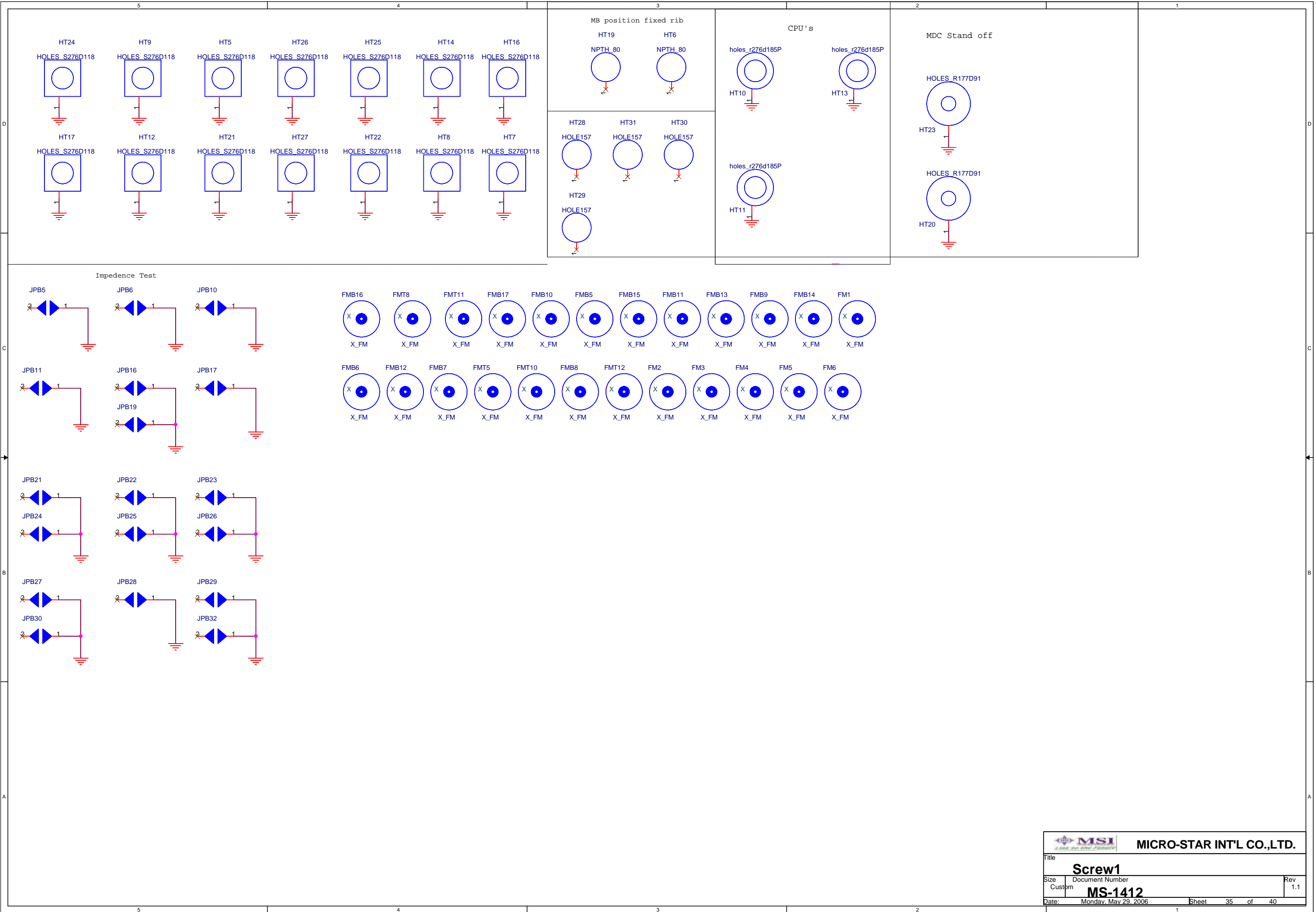
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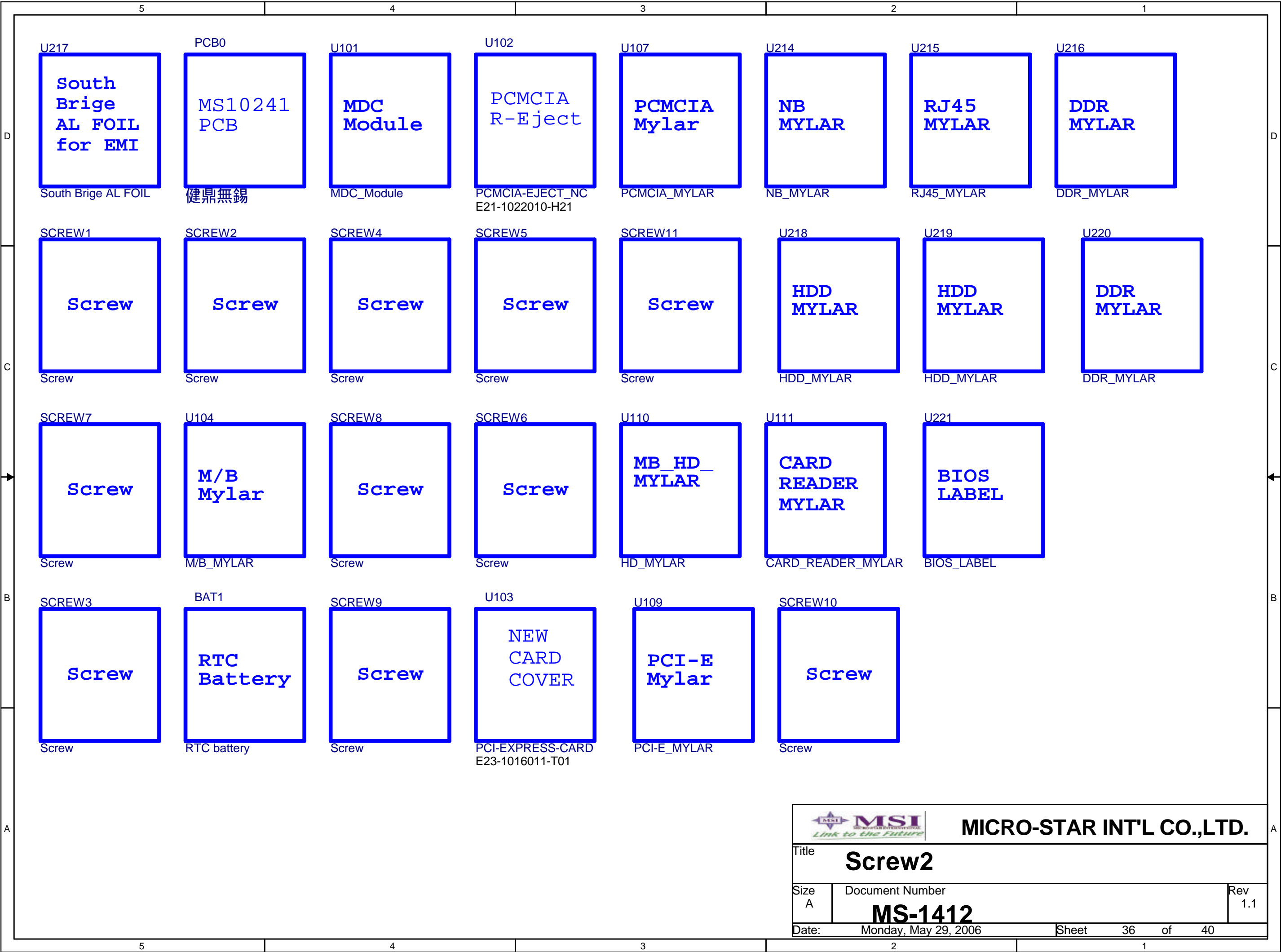




PR86 change to 5.6K ohm  
06'05'25 Able

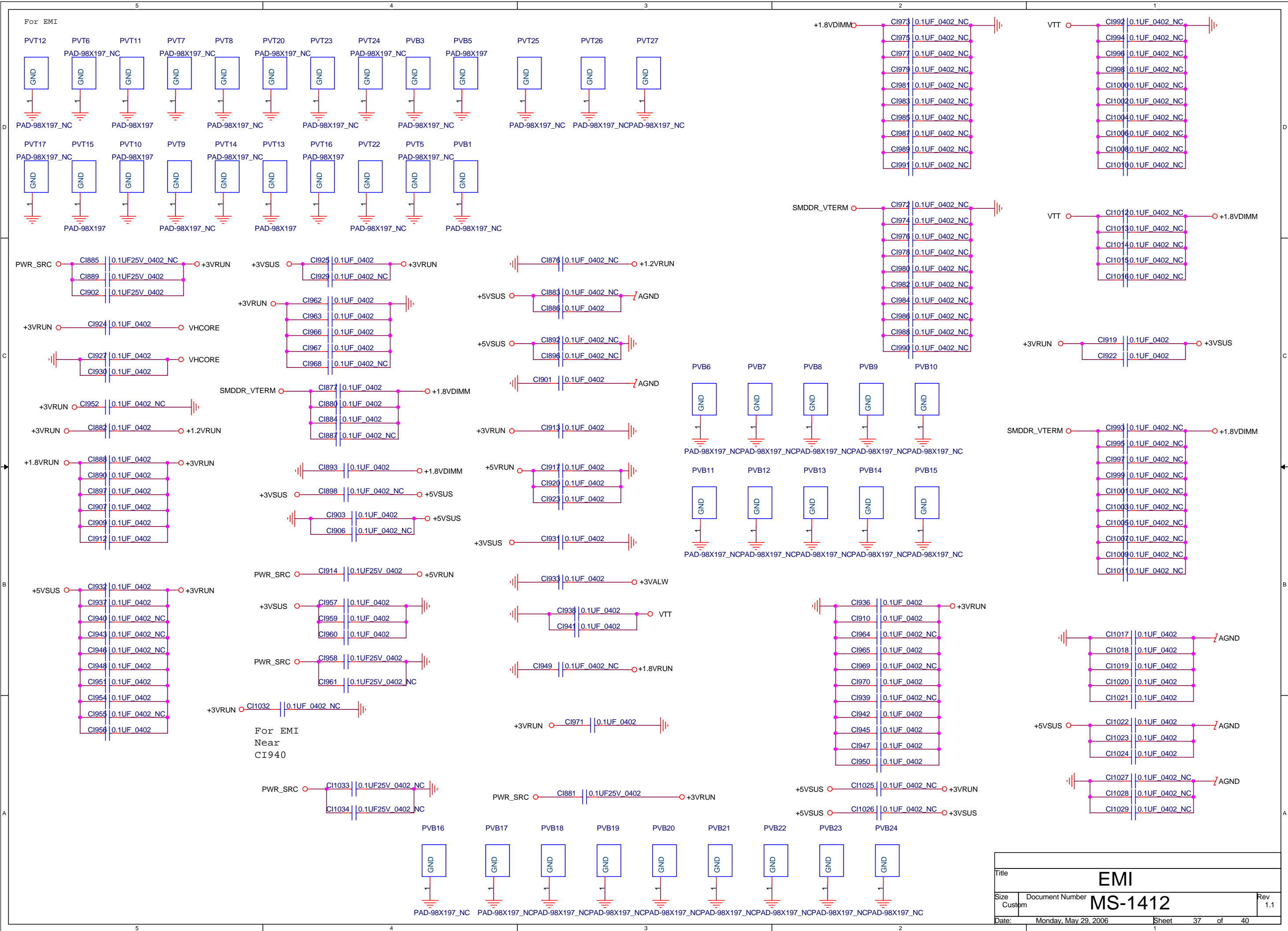
100 mil Trace list for layout  
DH1\_VCORE & DH2\_VCORE  
LX1\_VCORE & LX2\_VCORE  
DL1\_VCORE & DL2\_VCORE



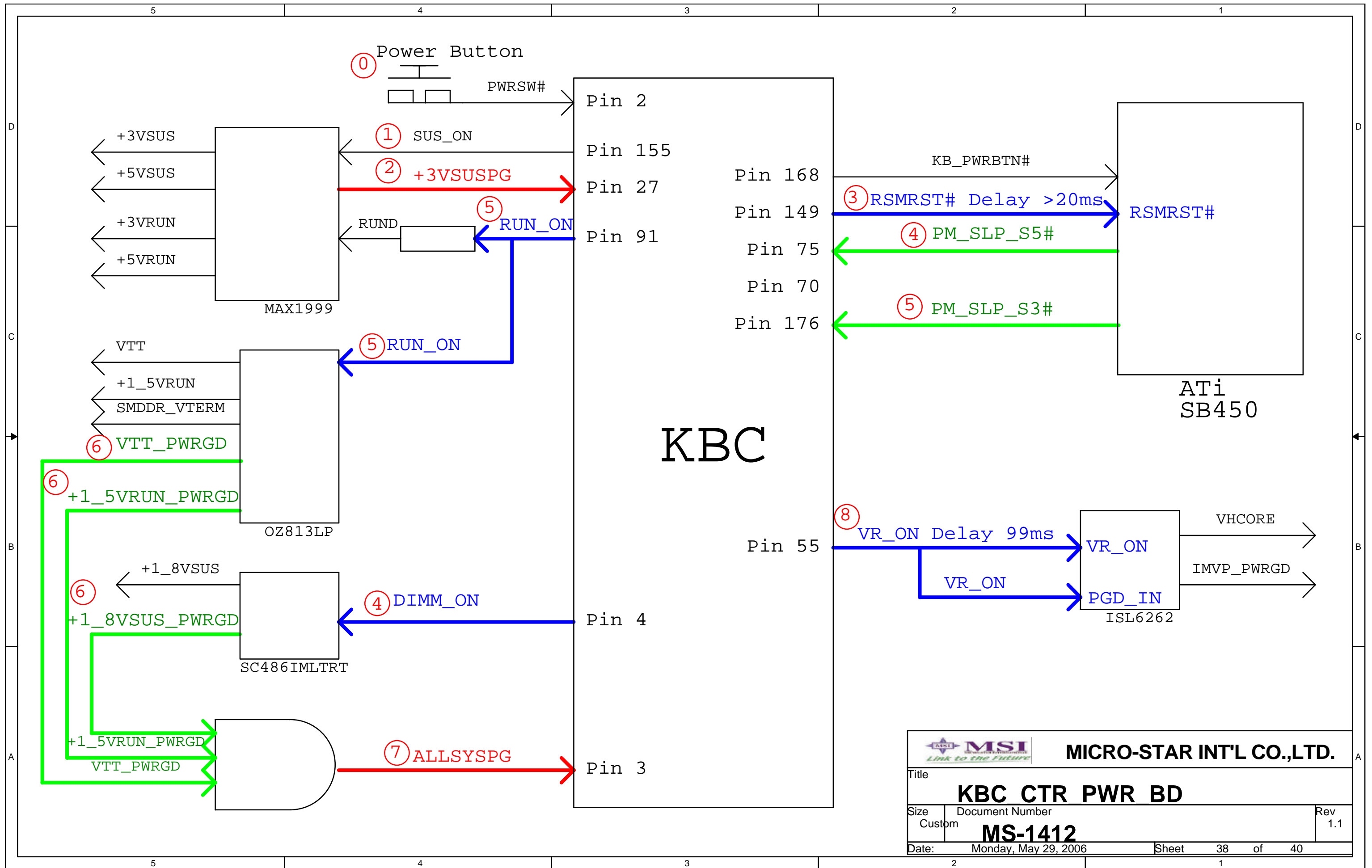


MICRO-STAR INT'L CO.,LTD.

Title			Screw2		
Size A	Document Number				Rev
	MS-1412				1.1
Date:		Monday, May 29, 2006			Sheet 36 of 40

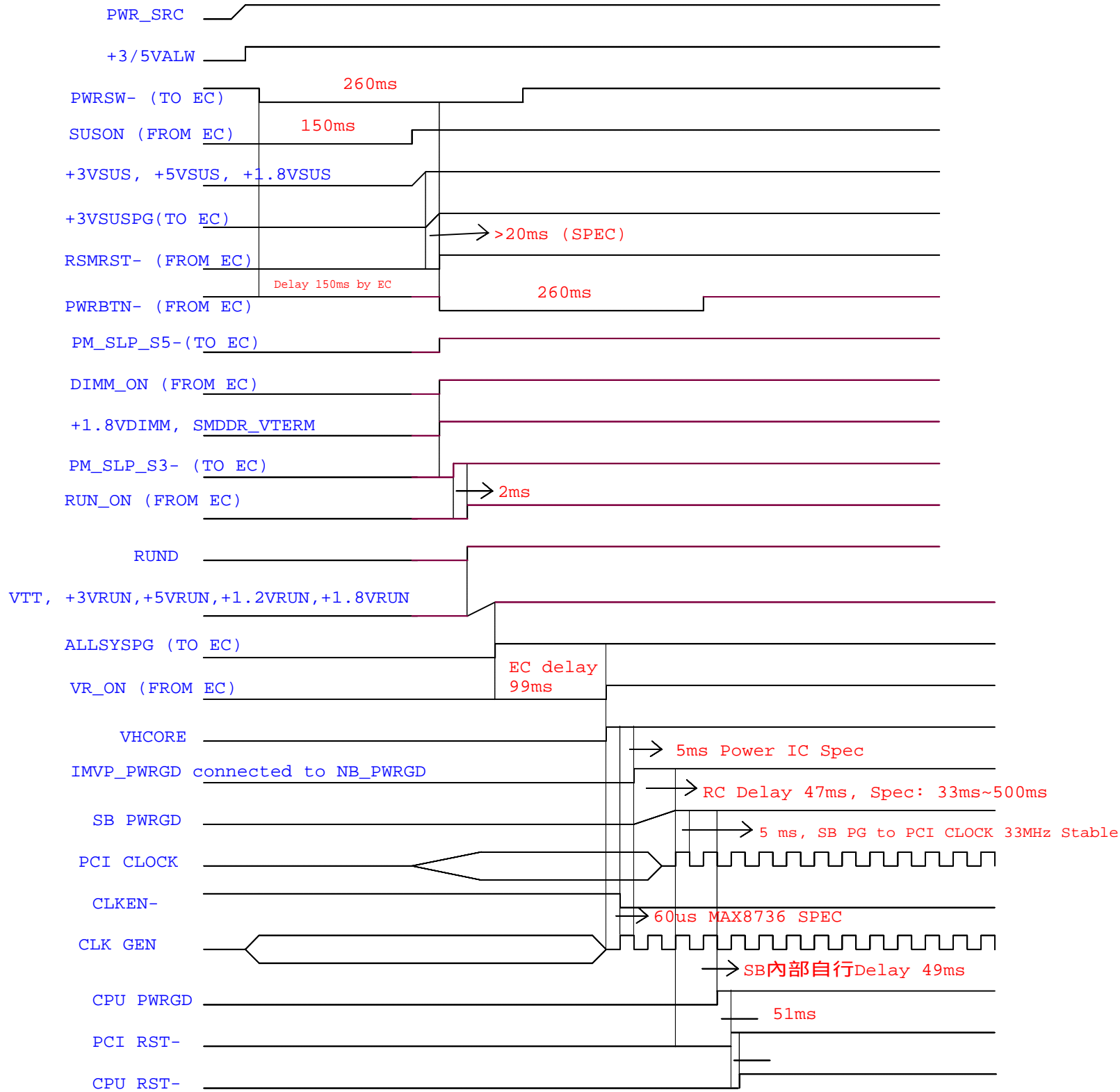


Title			EMI	
Size	Document Number	MS-1412		Rev
Custom				1.1
Date:	Monday, May 29, 2006	Sheet	37 of 40	

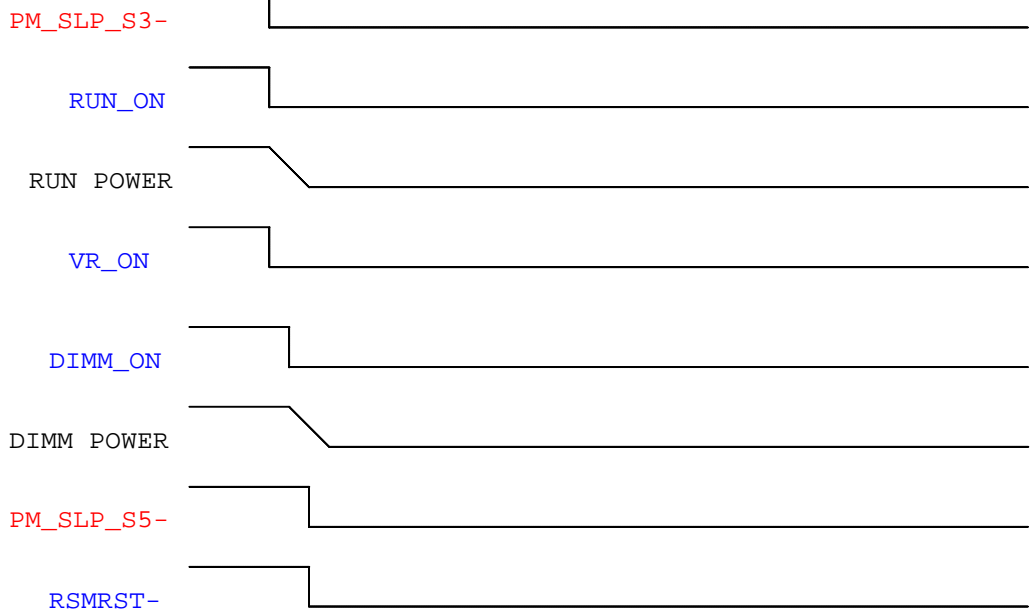




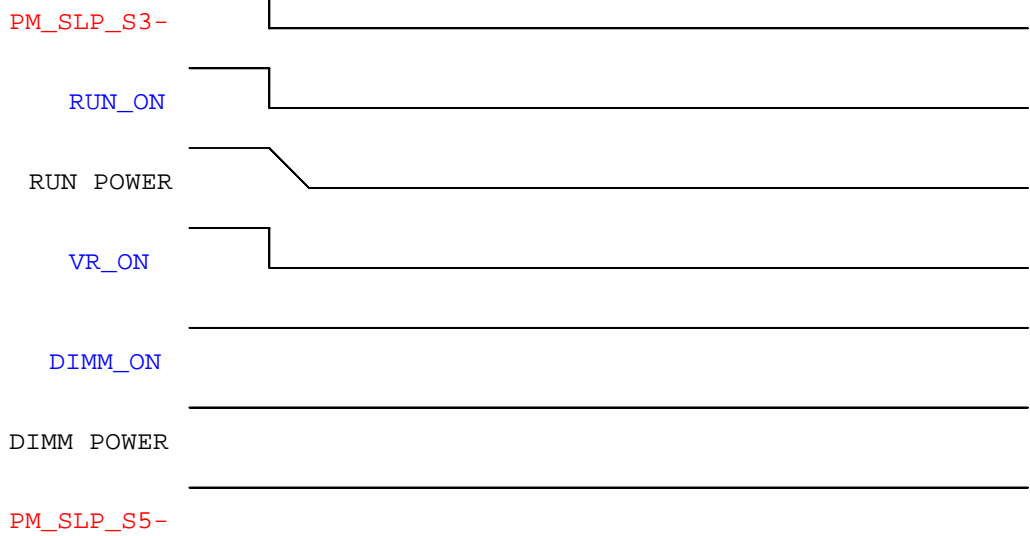
# Power Up



# Power Down



## S3



1.Y7,YT6 32.768MHZ change to D04-0300800-T16 for RoHS. Able 06'05'15

2.Y8 25MHz change to D04-1001100-T16 for RoHS. Able 06'05'15

3. 利用R955 or R956來決定LM86是吃+3VALW or +3VRUN. Able 06'05'25

4. Add R957用來做實驗。可調整阻值來量測RTC的耗電流。 Able 06'05'25